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Question Paper Code : 31315

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

Sixth Semester

Computer Science and Engineering

CS 2354/ CS 64/ 10144 CS 604 — ADVANCED COMPUTER ARCHITECTURE

(Regulation 2008/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is pipeline CPI?
2. What are the uses of static branch predictors?
3. What are the advantages of superblock approach?
4. What are the functional units of Itanium processor?
5. What are the advantages of MIMD multiprocessors?
6. What is the importance of memory consistency model?
7. What are the categories of cache organization based on placing a block?
8. What are the measures of I/O performance?
9. What is multicore?
10. What are the design issues of cell processor?

PART B — (5 × 16 = 80 marks)

11. (a) (i) What is Dynamic Scheduling? Explain how it is used to reduce data hazards. (8)

(ii) Explain how to reduce branch costs with dynamic hardware prediction. (8)

Or

(b) (i) Explain the various types of dependences in ILP. (8)

(ii) Explain in detail the concept involved in Instruction level parallelism. (8)

12. (a) (i) Distinguish between hardware versus software speculation mechanism in detail. (8)

(ii) Explain how the instruction format of IA64 is used to achieve the parallism. (8)

Or

(b) (i) Explain the trace scheduling in exploiting ILP. List its advantages. (8)

(ii) Briefly discuss the limitations of ILP. (8)

13. (a) (i) What do you mean by snooping protocol? Explain how it is used to maintain the coherence. (8)

(ii) Explain the different models of memory consistency. (8)

Or

(b) (i) Discuss the directory based cache coherence protocol. (8)

(ii) Explain how the hardware primitives can be used to build synchronization operations. (8)

14. (a) (i) Explain the various hit time reduction techniques. (8)

(ii) Explain the RAID architecture in detail. (8)

Or

(b) What are the categories of cache misses? Explain the various techniques available for reducing cache miss rate. (16)

15. (a) (i) Discuss the design challenges of SMT architecture. (8)

(ii) Explain the Intel multicore architecture with its benefits. (8)

Or

(b) (i) Explain in detail about the CMP architecture and its performance. (8)

(ii) Explain the architecture of IBM cell processor with neat block diagram. (8)

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