LIB
21/12/13 AN

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 31303

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

Fourth Semester

Computer Science and Engineering

CS 2253/CS 43/CS 1252 A/10144 CS 404/080250011– COMPUTER ORGANIZATION AND ARCHITECTURE

(Common to Information Technology)

(Regulation 2008/2010)

(Also Common to PTCS 2253 – Computer Organisation and Architecture for B.E (Part-Time) Third Semester – CSE – Regulation 2009)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is register indirect addressing mode? When is it used?

2. Differentiate between RISC and CISC.

3. Compare hardwired and micro programmed controls.

4. What is nano programming?

5. What is meant by data hazards in pipelining?

6. Define pipeline speedup.

7. Compare Static RAM and Dynamic RAM.

8. Define the terms hit, miss and ratio with respect to cache.

9. What is DMA? Mention its advantages.

10. What is meant by vectored interrupt?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain in detail the different instruction formats with examples. (8)

(ii) Explain ALU design. (8)

Or

(b) (i) Explain instruction sequencing in detail. (10)

(ii) What is the need for addressing modes? Explain any two types of addressing modes with examples. (6)

12. (a) Explain the following :

(i) Address sequencing in control memory. (8)

(ii) Micro program sequencer. (8)

Or

(b) (i) Explain multiple-bus organization. (8)

(ii) Explain the design of hardwired control unit. (8)

13. (a) (i) Describe the data and control path techniques in pipelining. (10)

(ii) Briefly explain the speedup performance models for pipelining. (6)

Or

(b) (i) What is instruction hazard? Explain in detail how to handle the instruction hazards in pipelining with relevant examples. (10)

(ii) Write note on exception handling. (6)

14. (a) (i) Explain the need for memory hierarchy technology, with a four-level memory. (6)

(ii) Explain the various mapping techniques associated with cache memories. (10)

Or

(b) (i) Explain a method of translating virtual address to physical address. (6)

(ii) What for replacement algorithms are used? Explain the important ones. (10)

15. (a) (i) Design a parallel priority interrupt hardware for a system with eight interrupt sources and explain. (8)

(ii) Explain USB interface. (8)

Or

(b) (i) Write a short note on I/O processor. (6)

(ii) What is the need for an I/O interface? Describe the functions of SCSI interface with a neat diagram. (10)

———————