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Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 75528

5 Year M.Sc. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

First Semester

Software Engineering

XCS 114/10677 SW 104 — DIGITAL PRINCIPLES

(Common to 5 Year M.Sc. Information Technology/M.Sc. Computer Technology)

(Regulation 2003/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. How are signed numbers represented in binary form?
2. Realise OR gate using only NAND gate.
3. Implement a full subtractor with two half subtractors and an external gate.
4. Using VHDL model a 2 to 1 Multiplexer.
5. How will you convert a JK – FF into a T-FF and D-FF?
6. What is the difference between latches and flip flops?
7. Draw the state diagram of a 2 bit up/down counter.
8. What is the difference between serial and parallel transfer?
9. Differentiate critical and non critical race.
10. How essential Hazards are caused?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Represent the decimal number 5136 in

(1) BCD

(2) Excess-3 code

(3) 2421 code and

(4) 6311 code. (6)

(ii) Convert the following numbers with the indicated bases to decimal:

(1) $(4310)_5$

(2) $(745)_8$

(3) $(525)_6$

(4) $(189)_{12}$. (6)

(iii) Convert the hexadecimal number 68BE to binary, and then convert it from Binary to Octal. (4)

Or

(b) (i) Express the function F(A,B,C,D) = D(A' + D) + B' D in a sum of minterms and a product of maxterms. (8)

(ii) State and prove De Morgan's theorem. (4)

(iii) Find the complement of the Boolean function (BC'+'A'D) (AB' + CD') and reduce them to a minimum number of literals. (4)

12. (a) (i) Simplify and implement the function

F (A,B,C,D) = A'B + A + C' + D' with NAND gates. (8)

(ii) Using k-Map simplify the Boolean function F using don't care condition d, in

(1) SOP and

(2) POS form.

$F(x,y,z) = \Sigma(2,3,4,6,7)$

$d(x, y, z) = \Sigma(0,1,5)$ (8)

Or

(b) (i) A combinational circuit is defined by the following two functions :

$F_1(x, y) = \Sigma(0,3)$

$F_2(x, y) = \Sigma(1, 2, 3)$

Implement the combinational circuit by means of the decoder and external NAND Gates. (8)

(ii) Explain the principles of decimal adder with suitable diagram. (8)

13. (a) Illustrate the procedure involved in state reduction in synchronous sequential logic with an example.

Or

(b) Explain the different flip flops with suitable logic circuit

14. (a) (i) Design a counter with the following binary sequence 0,1,3,2,6,4,5,7 and repeat. Use RS flip flops. (8)

(ii) Draw the diagram of a 4 bit binary ripple counter using flip flops that trigger on the positive edge. (8)

Or

(b) (i) Design a 4 bit Universal shift register and explain its operation. (8)

(ii) Model a SISO shift register using VHDL. (8)

15. (a) (i) Write an account of reduction of state in Asynchronous Sequential Circuit with a suitable example. (10)

(ii) Give the design procedure of Asynchronous Sequential Circuit. (6)

Or

(b) Show that dynamic hazards do not occur in two level AND-OR gate network.

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