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Question Paper Code : 75729

5 Year M.Sc. DEGREE EXAMINATION, JANUARY 2014.

First Semester

Software Engineering

ESE 012 — DIGITAL PRINCIPLES

(Regulation 2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State the uses of don't care conditions.
2. What will be the maximum number of outputs for a decoder with a 6 bit data word?
3. Define the term self-complementing code.
4. State two significant features of tabular method of minimization of boolean functions.
5. If the input frequency of a T flip – flop is 1600 KHz. What will be the output frequency?
6. How many flip-flops are required to build a counter of modulus 14 and modulus 8?
7. Comment on why parallel counter is faster than ripple counter.
8. Draw the logic diagram of three – bit ring counter.
9. How the hazards in combinational circuit can be removed?
10. List the different HDL descriptions of a design problem.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Realize the functions of NOT, AND, OR and NAND gates only with gates. (8)

(ii) Write short notes on

(1) Prime Implicates. (4)

(2) Computer aided minimization procedure. (4)

Or

(b) (i) Explain the following laws and theorems in detail:

(1) De Morgan's Theorem (2)

(2) Duality Theorem (2)

(3) Consensus Theorem (2)

(4) Covering law. (2)

(ii) Generate the parity bits for 8421 BCD code in an odd parity system. (8)

12. (a) (i) Design a 4 bit BCD to Excess – 3 code converter using binary parallel adder. (8)

(ii) Design a two – bit magnitude Comparator. (8)

Or

(b) Implement the function $Y(A,B,C,D)=\sum m$ (1, 4, 6, 7, 8, 9, 10, 11, 15) using 4 :1 MUX.

13. (a) A sequential circuit has four flip-flops ABCD and an input x is describe the following state equations. A (t + 1) = (CD' + CD) x + (CD + C'D') x'

B (t + 1) = A

C (t + 1) = B

D (t + 1) = C.

(i) Obtain the sequence of states when x = 1 starting from ABCD 0001.

(ii) Obtain the sequence of states when x = 0 starting from ABCD 0000.

Or

(b) Design a clocked sequential machine using T flip flop. Use state reduction if possible and also use straight binary state assignment.

14. (a) Design a mod – 5 synchronous counter using JK flip – flops with separate logic circuitry for each J and K input. Construct a timing diagram and determine the duty cycle of the output of the most significant stage.

Or

(b) Using SR flip-flops, design a synchronous counter which counts in the sequence 000,111, 101, 110,001,010, 000.

15. (a) (i) Design an asynchronous binary toggle circuit that changes state with each rising edge of clock input. Assume the initial output as zero.

(ii) State machine design using Moore model and mealy model.

Or

(b) Design an asynchronous sequential circuit using SR latch with two inputs A and B and one output y. B is the control input which, when equal to 1, transfers the input A to output y. when B is 0, the output does not change, for any change in input.
