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Question Paper Code : 82437

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

First Semester

VLSI Design

VL 9212/VL 912/10244 VL 104 – VLSI DESIGN TECHNIQUES

(Common to M.E. Applied Electronics, M.E. VLSI Design and Embedded Systems and M.E. Digital Electronics and Communication Engineering)

(Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define body effect in MOS transistor.
2. What is a pass transistor logic?
3. Draw the stick diagram for a BiCMOS 2-input NAND gate.
4. What is the significance of super buffers?
5. Differentiate between Clocked CMOS logic and CMOS domino logic.
6. Define gate to channel capacitance.
7. What is the significance of DRC and circuit extractors?
8. What is meant by sensitized path based testing?
9. List out the different models available in Verilog.
10. Write a program in data flow model for a full adder.

PART B — (5 × 16 = 80 marks)

11. (a) Differentiate between CMOS and Bipolar technologies. Also explain the Berkley n- well process.

Or

(b) Prove the following :

(i) Zpu/ Zpd for an nMOS inverter driven by another nMOS inverter is 4/1.

(ii) Zpu/ Zpd for an nMOS inverter driven by one or more pass transistors is 8/1.

12. (a) Draw the layout diagram for a 2 input CMOS NAND gate and briefly list out the CMOS Lambda-based design rules w.r.to it. Prove that Zpu/ Zpd for a Pseudo-nMOS NAND gate is 3/1.

Or

(b) Derive the expression for overall delay in a chain of connected pass transistors. A particular layer of MOS circuit has a resitivity of 1 ohm cm. A section of this layer is 55 μm long and 5 μm wide and has a thickness of 1 μm. Calculate resistance from one end of this section to the other (along the length).

13. (a) Explain the different factors used in scaling. What are the limitations of scaling?

Or

(b) Prove that sheet resistance is independent of the area of the conducting material. Discuss the rise time and fall time estimation for a CMOS inverter.

14. (a) Design a 4 bit serial right shift register. Draw the stick diagram for a CMOS type shift register.

Or

(b) Explain the design process involved to design a 4 bit arithmetic processor.

15. (a) What is a task? Give the syntax to declare and define a task. Write a program in Verilog to detect a sequence 1010 in behavioural model.

Or

(b) What is port mapping? Explain port mapping taking 4:1 multiplexer as an example.
