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**Question Paper Code : 82436**

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

First Semester

VLSI Design

VL 9211/VL 911/10244 VLE 13 — DSP INTEGRATED CIRCUITS

(Common to M.E. Applied Electronics and M.E. Medical Electronics)

(Regulation 2009/2010)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Compare the advantages of ASIC implementation with that of a DSP system based software implementation.
2. Determine the relationship between propagation delay, time constant and rise time for a first-order RC network.
3. Mention few applications using adaptive DSP algorithms.
4. Determine the transfer function of a system that is described by the difference equation.  
$$y(n) = b y(n - 1) + a x(n) . .$$
5. State necessary and sufficient condition for an FIR filter to have linear phase.
6. A two's complement number is multiplied by a factor of 0.5 and then quantized to the original word length. Determine the average value and the variance of quantization error.
7. State a suitable criteria for an ideal DSP architecture.
8. Define wave front arrays.
9. Multiply the binary integers corresponding to the decimal numbers  $(15)_{10}$  and  $(13)_{10}$  using Booth's algorithm.
10. Mention the useful property of two's complement representation of a number.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Describe the main features of a structured DSP design methodology. (8)
- (ii) Derive behavioural, data-flow and structured descriptions of a full adder. (8)

Or

- (b) Describe in detail the various VLSI process technologies. (16)

12. (a) A stable, causal digital filter has the following transfer function

$$H(z) = \frac{1.2z + 1.2}{z^2 - 1.6z + 0.63}$$

- (i) Determine the impulse response
- (ii) Determine the region of convergence
- (iii) Plot the pole-zero configuration in the z-plane
- (iv) Plot the magnitude response
- (v) Determine the step response. (16)

Or

- (b) (i) Determine the signal-flow graph for the FFT with  $N = 4$ , using decimation-in-frequency algorithm. What is the relationship between the decimation-in time and decimation-frequency algorithms?
- (ii) Show that the DFT for  $N = 8$  can be computed by essentially using two FTs with  $N = 4$ .

13. (a) (i) Determine the relation between the group delays of an analog filter and the corresponding digital filter that is obtained by bilinear transformation. (8)
- (ii) Design an interpolates that increases the sampling frequency with a factor two, from 1.6 MHz to 3.2 MHz. The energy of the input signal is contained within the band 0 to 680 kHz. No signal is noises present above this band. The input data word length is 12 bits and output signal should have essentially the same accuracy. (8)

Or

- (b) (i) Show that a two-port adaptor is pseudo-loss less. (8)
  - (ii) Show that the quantization scheme will suppress parasitic oscillations. (8)
14. (a) (i) What are main limitation in shared memory architecture? Discuss different approaches in overcoming or reducing these limitations. (8)
- (ii) Illustrate the basic principle of systolic array architecture with a suitable example. (8)

Or

- (b) Describe the major steps in a systematic approach to implementing DSP algorithms into an ASIC. Justify that it is the optimal approach.
15. (a) (i) Show that the negative value of a number  $x$ , in two's complement representation can be obtained by inverting all bits in the binary word and adding. (8)
- (ii) Describe the structure of tree-based and array multiplier. (8)

Or

- (b) Using a bit-serial PE based on serial/parallel multiplier implement the following :

  - (i) Direct form FIR filter with fixed coefficient (8)
  - (ii) Transposed direct form FIR filter with fixed coefficient. (8)