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Question Paper Code : 82448

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

Elective

VL 9257/VL 957/10244 VLE 41 – PHYSICAL DESIGN OF VLSI CIRCUITS

(Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is the difference between MPGA and FPGA?
2. List the advantages of packaging?
3. Define portitioning.
4. Define the cost function in placement.
5. What do you mean by local routing?
6. What is Steiner tree?
7. Define clock skew.
8. Draw the lumped circuit approximations for distributed L Model.
9. Define dogleg.
10. What is the difference between PAL and PLA?

PART B — (5 × 16 = 80 marks)

All questions carry equal marks.

11. (a) (i) List the various processing steps involved in MOS design. (8)

(ii) Compare the various layout styles and architectures. (8)

Or

(b) (i) Discuss in detail about Layout Rules and circuit abstraction. (8)

(ii) Write about the efficient algorithmic techniques used for VLSI layout. (8)

12. (a) (i) Design an algorithm for transforming a hypergraph into a graph. Discuss effectiveness of your technique as it applies to the bipartition problem. (8)

(ii) Explain the floorplanning concept based on simulated annealing. (8)

Or

(b) (i) Prove that there is a one to one correspondence between a sliceable floorplan and a normalized polish expression. (8)

(ii) Explain about Iterative force-directed algorithms. (8)

13. (a) (i) Prove that the total weight of a minimum-spanning tree in an edge weighted graph is at most two times the length of an optimal Steiner tree in the same graph. (8)

(ii) Design a greedy algorithm to order the channel in a given placement so as to minimize the number of switchboxes. (8)

Or

(b) (i) Briefly describe the various Steiner minimal tree (SMT) algorithms used for global routing. (8)

(ii) Route the following channel consisting of 11 columns using the left edge algorithm where 0 indicates an empty position.

TOP = 3 4 0 1 2 4 3 5 2 1 0

BOT = 1 0 3 0 4 0 5 2 1 5 4 (8)

14. (a) (i) Explain in detail about the models for the interconnect delay. (8)

(ii) With neat sketches explain constrained via minimization problem. (8)

Or

(b) (i) Design an algorithm with bounded delay and small skew, using the linear delay model. (8)

(ii) With neat sketches explain unconstrained Via Minimization problem. (8)

15. (a) (i) Explain in detail about merging in Planar Subset Problem (PSP) with fixed number of modules. (8)

(ii) List all possible routing requirements for Multi Chip Modules (MCM) (8)

Or

(b) (i) Explain about Wire-Length minimization technique for single-layer routing. (8)

(ii) Write in detail about the six basic steps in Over the Cell (OTC) Routing. (8)
