LIB
4/12/13 FN

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 82447

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

Elective

VLSI Design

VL 9256/VL 956/10244 VLE 32 — VLSI TECHNOLOGY

(Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State the reasons for the choice of SiO_2 in IC processing.
2. What are the methods of water cleaning?
3. What is lithography?
4. State any two properties of plasmas.
5. What is divacancy?
6. What is patterning?
7. What is latch-up problem?
8. State the continuity equation and its significance.
9. State the uses of TEM and SEM.
10. State the different types of IC packaging.

PART B — (5 × 16 = 80 marks)

11. (a) Explain an oxidation technique. Discuss briefly on oxidation inducted defects.

Or

(b) (i) Write notes on silicon on insulators. (8)

(ii) Explain Czochralski crystal growing process. (8)

12. (a) (i) Explain electron lithography procedure. (8)

(ii) Explain briefly an isotropic etching mechanism. (8)

Or

(b) (i) Explain the reactive plasma etching technique. (8)

(ii) Compare the performance of optical lithography, X-ray lithography, electron lithography and ion-lithography. (8)

13. (a) (i) Explain Flick's one dimensional diffusion equation. (8)

(ii) Explain briefly physical vapour deposition. (8)

Or

(b) (i) Explain the working of ion implantation set up. (8)

(ii) Explain about the crystallographic damage that arises during ion implantation. How can it be rectified? (8)

14. (a) Explain the simulation of etching and deposition processes.

Or

(b) Explain in detail, the fabrication of CMOS transistor.

15. (a) Discuss briefly about the interactions of analytical beams with materials used in VLSI technology.

Or

(b) Explain the design considerations to be followed during packaging of ICs.

———————