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Question Paper Code : 81325

M.E./M.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

First Semester

Computer Science and Engineering

CS 9211/CS 911/10244 CS 105 – COMPUTER ARCHITECTURE

(Common to M.Tech. Information Technology)

(Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What do you mean by pipelining?
2. State Amdahl's Law.
3. What is branch-target buffer and what are the uses it?
4. What are the advantages and limitations of Tomasulo's approach?
5. What are the advantages of hardware-based speculation over dynamic scheduling?
6. Compare dynamic branch prediction and static branch prediction.
7. What is false sharing and when does it occur?
8. What is multi-core architecture?
9. Define I/O bandwidth and I/O throughput.
10. How does cache memory improve the system performance?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Discuss about the major factors that influence the cost of a computer and how these factors are changing overtime. (8)

(ii) Explain the structure of pipeline processor and mention the advantages and disadvantages of designing a floating-point processor in the form of a k-stage pipeline. (8)

Or

(b) (i) Explain multi-cycle pipeline operation in detail. (8)

(ii) What is ISA? Describe the classification of instruction set architecture in detail. (8)

12. (a) (i) Summarize the primary approaches in use for multiple-issue processors and their characteristics (7)

(ii) Explain the basic structure of a MIPS floating-point unit using Tomasulo's algorithm and explain the Tomasulo's algorithm to overcome the hazards with dynamic scheduling. (9)

Or

(b) Explain briefly how the following techniques were used to exploit the instruction level parallelism:

(i) Dynamic scheduling (8)

(ii) Speculation (8)

13. (a) Briefly describe the compiler techniques for exposing instruction level parallelism. (16)

Or

(b) Briefly describe the hardware support for exploiting more parallelism. (16)

14. (a) (i) Explain the mechanism for implementing snooping protocols in details. (10)

(ii) Explain the architecture of a multi-core processor with neat diagram. (6)

Or

(b) (i) Discuss about the operating system impact on SMT architecture. (6)

(ii) What is SMT and what applications benefits from SMT processor? Explain the architecture of a typical SMT processor in detail. (10)

15. (a) (i) Explain various cache optimization techniques in detail. (10)

(ii) Describe the steps involved in designing and evaluating and I/O system. (6)

Or

(b) (i) What is RAID? Explain the standard RAID levels and summarizes the pros and cons of each level. (8)

(ii) Discuss about the techniques for improving memory performance. (8)
