**A** **Reg. No. :** | | | | | | | | | | |

# Question Paper Code: 53306

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2018

Third Semester

Electrical and Electronics Engineering

15UEE306 -DIGITAL LOGIC CIRCUITS

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. After counting 0, 1, 10, 11, the next binary number is CO1-U

   (a) 12 (b)100 (c)101 (d)110

2. The expansion of ECL is CO1- R

   (a) Emitter-collector logic (b) Emitter-complementary logic

   (c) Emitter-coupled logic (d) Emitter Common logic

3. A combinational circuit that selects one from many inputs CO2- U

   (a) Encoder (b) Decoder (c) Demultiplexer (d) Multiplexer

4. Full adder has CO2- R

   (a) 1 inputs (b) 2 inputs (c) 3 inputs (d) 4 inputs

5. When both inputs are high, then output of JK flip-flop will be CO3-U

   (a) 0 (b) 1 (c) No change (d) Toggle

6. Flip-flop outputs are always CO3-U

   (a) Complimentary (b) Same

   (c) Independent of each other (d) Same as previous input

7. Output state in asynchronous sequential logic circuit changes when CO4-U

(a) Input changes (b) Clock pulse is high

(c) Input and clock pulse change (d) Clock pulse is low

8. PAL has CO4- R

(a) Fixed AND array and Fixed OR array

(b) Fixed AND array and Programmable OR array

(c) Programmable AND array and Fixed OR array.

(d) Programmable AND array and Programmable OR array.

9. VHDL stand for CO5- R

(a) Verilog hardware description language

(b) VHSIC hardware description language

(c) Very hardware description language

(d) VMEbus description language

10. Each unit to be modeled in a VHDL design is known as CO5- R

(a) Behavioural model (b) Design architecture

(c) Design entity (d) Structural model

PART – B (5 x 2= 10 Marks)

11. Write the advantages of Gray code over other binary codes. CO1- U

12. Compare minterms and maxterms in Boolean functions. CO2- U

13. Write the truth table for T flipflop. CO3- R

14. Differentiate Static – 1 and Static – 0 hazards. CO4- R

15. List the different modeling techniques available in VHDL programming. CO5- R

PART – C (5 x 16= 80 Marks)

16. (a) (i) Construct the hamming code for the information code $1011_2$ by using odd parity. CO1-C (12)

(ii) Convert $152_{10}$ to its equivalent binary, octal and hexadecimal value. CO1-App (4)

Or

(b) (i) Convert $1100101_2$ to its equivalent decimal, octal and hexadecimal value. CO1-App (4)

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|---|---|---|---|---|
| | | (ii) Discuss the features and characteristics of TTL, ECL and CMOS logic families. | CO1-U | (12) |
| 17. | (a) | (i) Minimize the following Boolean expression using K-map and realize it using the basic gates. $Y = \Sigma_m (1,3,5,9,11,13)$ | CO2-App | (12) |
| | | (ii) Write the limitations of K-Map in minimizing the Boolean functions. | CO2-U | (4) |
| | | Or | | |
| | (b) | (i) Design and realize full adder using basic logic gates. | CO2-App | (8) |
| | | (ii) Design and realize 4:1 multiplexer using basic logic gates. | CO2-App | (8) |
| 18. | (a) | Design and describe the operation of bidirectional shift register. | CO3-Ana | (16) |
| | | Or | | |
| | (b) | Design and realize 3 bit UP mode synchronous counter using JK flip-flops. | CO3-C | (16) |
| 19. | (a) | (i) Design an Asynchronous sequential circuit with two inputs x1 and x2 and with one output z. Initially both inputs are equal to zero. When x1 changes from 0 to 1,then Z = 1 and when x2 changes from 0 to 1, then Z = 0 and Z=0 otherwise. | CO4-C | (12) |
| | | (ii) Compare fundamental mode and pulse mode in asynchronous sequential logic circuits. | CO4-U | (4) |
| | | Or | | |
| | (b) | Realize the following Boolean functions using PLA and PAL. $Y_1 = \Sigma_m (1,2,4,5,6)$ , $Y_2 = \Sigma_m (0,1,6,7)$ , $Y_3 = \Sigma_m (2,6)$ | CO4-C | (16) |
| 20. | (a) | (i) Compare Sequential programming and concurrent programming. | CO5-U | (4) |
| | | (ii) Illustrate RTL design using VHDL with the help of an example. | CO5-Ana | (12) |
| | | Or | | |
| | (b) | (i) Write a HDL code for realizing JK FF in behavioral modeling. | CO5-C | (8) |
| | | (ii) Write a HDL code for realizing half adder in behavioral modeling. | CO5-C | (8) |

**53306**