Reg. No. : | | | | | | | | | | |

Question Paper Code: 43306

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2018

Third Semester

Electrical and Electronics Engineering

14UEE306 – DIGITAL LOGIC CIRCUITS

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. The 2's complement of the number 1010101 is

   (a) 0101011 (b) 0101010 (c) 1101010 (d) 1110011

2. What is the major advantage of ECL logic?

   (a) very high speed (b) wide range of operating voltage
   (c) very low cost (d) very high power

3. The output of an exclusive-NOR gate is 1. Which input combination is correct?

   (a) A=1, B=0 (b)A=0, B=1 (c) A=0, B=0 (d) none of these

4. AND-OR realization is equivalent to

   (a) SOP (b) POS (c) K-map (d) None of these

5. Race around condition occurs in JK flip-flop if

   (a) J=1,K=1 (b) J=0,K=0 (c) J=0,K=1 (d) J=1,K=0

6. In the toggle mode a JK flip-flop has

(a) J = 0, K = 0 (b) J = 1, K = 1 (c) J = 0, K = 1 (d) J = 1, K = 0

7. Which of the following is a type of shift register counter?

(a) Decade (b) Binary (c) Ring (d) BCD

8. What programmable technology is used in FPGA devices?

(a) SRAM (b) FLASH (c) Antifuse (d) All the above

9. The example of sequential circuit is

(a) Counter (b) 7-segment display
(c) Combinational logic circuit (d) Shift register

10. A full-adder h.as a $C_{in} = 0$. What are the sum $(\sum)$ and the carry (C_{out}) when A = 1 and B = 1?

(a) $\sum = 0, C_{out} = 0$ (b) $\sum = 0, C_{out} = 1$
(c) $\sum = 1, C_{out} = 0$ (d) $\sum = 1, C_{out} = 1$

PART - B (5 x 2 = 10 Marks)

11. State DeMorgan's theorem.

12. Why is MUX called as data selector?

13. What are synchronous sequential circuit?

14. What is a hazard?

15. Write VHDL code for D flip-flop.

PART - C (5 x 16 = 80 Marks)

16. (a) (i) Explain Gray code and Binary code. (8)

(ii) Compare the Characteristics of TTL, ECL and CMOS logic families. (8)

Or

(b) (i) Convert 1010111011101100_2 into octal, decimal and hexadecimal equivalent. (8)

(ii) Explain Hamming code with an example. State its advantages over parity codes. (8)

17. (a) Design a full adder using two half-adders and an OR gate. (16)

Or

(b) (i) Design a BCD to Excess-3 code converter. (8)

(ii) Design a full adder and implement it using suitable multiplexer. (8)

18. (a) Design a synchronous counter to count the sequence 0 - 1 - 2 - 4 5 - 6 - 0 using JK flip flop. (16)

Or

(b) (i) Design a serial adder using Mealy state model. (8)

(ii) List and explain the steps used for analyzing a synchronous sequential circuit. (8)

19. (a) Explain the various types of hazards in sequential circuit design and methods to eliminate them. Give suitable examples. (16)

Or

(b) (i) An asynchronous sequential circuit is described by the following excitation and output function.

$Y=x_1\ x_2'+(x_1 + x_2')y$

$Z=y$

(1) Draw the logical diagram of the circuit

(2) Derive the transition table and output map.

(3) Obtain flow table. (8)

(ii) Implement the following function using PLA $F_1 = \sum m (4,5,7)$ and

$F_2 = \sum m (3,5,7)$. (8)

20. (a) Explain the structural VHDL description for a 2 to 4 decoder in details. (16)

Or

(b) Explain RTL design using VHDL with the help of examples. (16)