	С	Reg. No. :											
Question Paper Code: 53402													
B.E. / B.Tech. DEGREE EXAMINATION, NOV 2018													
Third Semester													
Electronics and Communication Engineering													
15UEC302 - DIGITAL ELECTRONICS AND DESIGN													
(Regulation 2015)													
Dur	ation: Three hours							Ma	ximu	ım: 1	00 N	Aark	S
	Answer ALL Questions												
		PART A - (5 x	x 1 =	= 5 N	larks	s)							
1.	Which of the following expressions is in the sum-of-products (SOP)CO1-Uform?							1- U					
	(a) $(A + B)(C + D)$	(b) (A)B(CD)	(0	e) AI	B(CI))			((d) A	B +	CD	
2.	How many 3-line-to-8-line decoders are required for a 1-of-32 CO2 decoder?						2- R						
	(a) 1	(b) 2	(0	c) 4					((d) 8			
3.	A ripple counter's speed is limited by the propagation delay of CO.						3- R						
	(a) Each flip-flop (b)					(b) All flip-flops and gates							
	(c) The flip-flops only	with gates	(0	l) Oı	nly c	ircui	t gate	es					
4.	The time sequence of enumerated in a	of inputs, outputs, a	ınd	flip	flop	stat	tes c	an l	be			CO	4- R
	(a) Transition table	(b) Truth table	(0	c) Cł	narac	teris	tic ta	ble	((d) N	one	of tł	iese
5.	PALs tend to execute	logic.										CO)5-R
	(a) SAP	(b) SOP	(0	e) PL	A				((d) S	PD		

PART – B (5 x 3= 15 Marks)

6.	Sim	plify the following using De Morgan's theorem [((AB)'C)" D]'.	CO1- Ana					
7.	Wha	at is binary decoder?	CO2- R					
8.	Def	ine skew and clock skew.	CO3- R					
9.	Give	e the comparison between synchronous and asynchronous counters.	CO4- R					
10.	Wha	at is programmable logic array? How it differs from ROM?	CO5- R					
		PART – C (5 x 16= 80 Marks)						
11.	(a)	Simplify the following function using $K - map$, Y = A'B'C+ABC'D'+A'BD+ABCD'and implement the function using logic gates.	CO1- App	(16)				
		Or						
	(b)	Minimize the given Boolean function using Quine McCluskey Method	CO1- App	(16)				
		$F(A,B,C,D) = \sum (0, 2, 3, 6, 7, 8, 10, 12, 13)$						
12.	(a)	Design and implement the conversion circuits for BCD to $Excess - 3$ code.	CO2- App	(16)				
	Or							
	(b)	(i) Draw the logic diagram of a 2-bit by 2-bit binary multiplier and explain its operation.	CO2- U	(8)				
		(ii) Realize F(w, x, y, z)= Σ (1,3,4,11,12,13,14,15) using 8 to 1 Mux.	CO2- App	(8)				
13.	(a)	Design an asynchronous BCD ripple counter using JK flip – flop. Or	CO3- App	(16)				
	(b)	Design a 4 bit Synchronous Binary counter and explain its operation.	CO3- App	(16)				
14.	(a)	(i) Design a sequential circuit with two D flip-flops A and B and an input x. when $x=0$ the state of the circuit remains the same. When the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00 and repeats.	CO4- Ana	(8)				

(ii) Explain the static and dynamic hazards in combinational logic CO4- U (8) circuits with an example.

Or

- (b) Design a primitive flow table for a circuit with two inputs x1 and CO4- Ana (16) x2 and two outputs z1 and z2 that satisfies the following four conditions.
 - (i) When $x_1x_2 = 00$ output $z_1z_2 = 00$.
 - (ii) When $x_1 = 1$ and x2 changes from 0 to 1, the output $z_1z_2 = 01$.
 - (iii) When $x_2 = 1$ and x_1 changes from 0 to 1, the output $z_1z_2 = 10$.
 - (iv) Otherwise the output does not change.

15. (a	(a)	Implement the binary to excess-3 code converter using ROM.	CO5- App	(16)
	(b)	(i) Implement Boolean function with PLA:	CO5- App	(10)
		$F1(A, B, C) = \sum (0, 2, 3, 4)$ and $F2(A, B, C) = \sum (1, 5, 6, 7)$		
		(ii) Compare the static and dynamic RAMs.	CO5- U	(6)