**Reg. No. :** | | | | | | | | | | |

## Question Paper Code: 43402

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2018

Third Semester

Electronics and Communication Engineering

14UEC302 – DIGITAL ELECTRONICS AND DESIGN

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. The equivalent hexadecimal of binary number 1011101.1011 is

   (a) B33 (b) EFF2.F (c) 5 D.B (d) 4A.67

2. Universal gates are

   (a) NAND and AND gates (b) NOR and OR gates

   (c) NAND and NOR gates (d) AND and OR gates

3. A circuit with many inputs and only one output is called

   (a) de multiplexer (b) decoder (c) half adder (d) multiplexer

4. A device that convert from decimal to BCD is

   (a) decoder (b) encoder (c) multiplexer (d) demultiplexer

5. Which latch is called a transparent latch

   (a) SR latch (b) JK latch (c) D latch (d) T latch

6. The characteristic equation of D-flip-flop

   (a) $Q(t + 1) = D + 1$ (b) $Q(t + 1) = D$

   (c) $Q(t + 1) = D'$ (d) $Q(t + 1) = D'Q$

7. CMOS fan out depends on

(a) Power dissipation (b) Propagation delay

(c) Current (d) Noise margin

8. The limit of a noise voltage which may be allowed in the circuit is

(a) Noise Margin (b) Noise Voltage

(c) Low level input noise (d) High level input noise

9. Sequential circuit output depends on

(a) present input and feedback path (b) past input only

(c) present input only (d) none of the above

10. The number of state variable '*m*' produces

(a) $2^{m+1}$ states (b) $2^{m-1}$ states (c) $2^{m}$ states (d) None

PART - B (5 x 2 = 10 Marks)

11. Implement 2 input Ex-OR gate using NAND gate.

12. With truth table draw the circuit of 3-bit odd parity generator.

13. State the drawbacks of RS flip flop.

14. How does a static RAM differ from dynamic RAM?

15. What arte advantages of merging process?

PART - C (5 x 16 = 80 Marks)

16. (a) Simplify the following expression using Quine Mccluskey method
f [ w, x, y , z ] = ∑ ( 0, 2, 3, 5, 6, 7, 8, 9 ) + d ( 10, 11, 12, 13, 14, 15)
Realize the minimized function using NOR gates only. (16)

Or

(b) Consider the minimization of the following switching function using the QUINE-McCLUSKEY method. $F(x_1, x_2, x_3, x_4)=\sum(0, 5, 7, 8, 9, 10, 11, 14, 15)$. (16)

17. (a) (i) Construct the full adder using two half adders. (4)

(ii) Explain about the 4x1 multiplexer and Implement the function
*F (A, B, C)* = ∑(1, 3, 5, 6) using a multiplexer. (12)

Or

(b) Design 4 bit Binary to BCD code converter. (16)

18. (a) Explain the working of 3-bit universal shift register with neat block diagram. (16)

Or

(b) Explain synchronous decade counter using T flip flop. (16)

19. (a) Briefly explain about PLD's with a suitable example. (16)

Or

(b) Explain synchronous decade counter using T flip flop. (16)

20. (a) Design a sequence detector circuit that produces an output 1 whenever the sequence 101101 is detected. (16)

Or

(b) Design serial binary adder using D-flip-flop. (16)

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