C Reg. No. : | | | | | | | | | | |

Question Paper Code: 56403

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2018

Sixth Semester

Electronics and Communication Engineering

15UEC603- VLSI DESIGN

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (5 x 1 = 5 Marks)

1. The syntax for gate instantiation with the delay specification is CO1- R

   (a) gate_type [delay] [instance name] (terminal_list);

   (b) gate_type [instance name] [delay] (terminal_list);

   (c) gate_type [delay] (terminal_list) [instance name];

   (d) gate_type (terminal_list) [delay] [instance name];

2. MOS device is --------- CO2- R

   (a) Voltage controlled switch (b) Current controlled switch

   (c) Capacitance Controlled switch (d) Inductance controlled switch

3. The resistance and capacitance product of the MOS transistor is called CO3- R

   (a) intrinsic delay (b) intrinsic delay (c) botha&b (d) none

4. TG function is similar to CO4- R

   (a) Analog switch (b) digital switch (c) relay (d) SCR

5. Stuck at 0 and stuck at 1 faults are called as -------- respectively CO5- R

   (a) SA1 and SA0 (b) SA0and SA1 (c) all of these (d) none

PART – B (5 x 3= 15Marks)

6. What are the value sets in Verilog? CO1- R

7. Compare NMOS and PMOS. CO2- R

8. What are the factors that cause the static power dissipation in cross circuits? CO3- Ana

9. Define tpd & tcd.. CO4- R

10. What is Iddq testing? CO5- U

PART – C (5 x 16= 80Marks)

11. (a) Design a adder to add two data each having 4 bits using Ex-or gate and And gate . Assume that 4 full adders are connected in serially, one Full adder waits for the carry input from the previous adder CO1- Ana (16)

Or

(b) (i) Design a 3:8 decoders with case statements using verilog HDL. CO1- Ana (8)

(ii) Design a ripple carry adder using verilog HDL. CO1- Ana (8)

12. (a) Explain about the Silicon On Insulator(SOI) CMOS processing Technology in detail. CO2- Ana (16)

Or

(b) Illustrate and explain the CMOS transistor fabrication step. Consider p – type silicon is used as substrate (wafer) and the p – substrate is used for nMOS transistor and to create n-well for pMOS transistor. CO2- App (16)

13. (a) Assume a 180 nm standard cell process can have an average switching capacitance of 150pF/mm^2. It has the activity factor of 0.1. Estimate the power consumption of the chip if it has the area of 70mm^2 and runs at 450MHz at Vdd=0.9V. Analyze the dynamic power consumption if Vdd is increased to 5V and and switching frequency reduced to 300MHz respectively. CO3- Ana (16)

Or

(b) (i) Discuss yield and reliability in CMOS technology. CO3- U (8)

(ii) What is charge sharing? Explain it with an example. CO3- U (8)

14. (a) Design a EX – OR gate and EX – NOR Gate using CMOS logic CO4- App (16)

Or

	(b)	Design a combinational circuit which should select one input among 8 inputs with transmission gates .	CO4- U	(16)
15	(a)	Explain in detail about scan based approaches for CMOS testing..	CO5- U	(16)
		Or		
	(b)	(i) Design a 3- bit pseudo random sequence generator using LFSR for BIST.	CO5- Ana	(8)
		(ii) Construct a BILBO by using the pattern generator and signature analyzer.	CO5- Ana	(8)

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