Reg. No. : | | | | | | | | | | |

Question Paper Code: 46404

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2018

Sixth Semester

Electronics and Communication Engineering

14UEC604-VLSI DESIGN

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

(Smith chart may be permitted)

PART A - (10 x 1 = 10 Marks)

1. VLSI technology uses _____to form integrated circuit.

   (a) Transistors (b) Switches (c) Diodes (d) Buffers

2. The difficulty in achieving high doping concentration leads to

   (a) Error in concentration (b) Error in variation
   (c) Error in doping (d) Distribution

3. In accordance to the scaling technology , the total delay of the logic circuit depends on

   (a) The capacitor to be charged
   (b) The voltage through which capacitance must be charged
   (c) Available current
   (d) All of the above

4. The time needed for an output to change as the result of an input change is known as

(a) noise immunity (b) fanout (c) propagation delay (d) rise time

5. In CMOS circuits, which type of power dissipation occurs due to switching of transient current and charging and discharging of load capacitance?

(a) Static dissipation (b) Dynamic dissipation
(c) Both (a) and (b) (d) None of these

6. The sequential circuit is also called

(a) Flip-flop (b) Latch (c) Strobe (d) None of the Mentioned

7. Boundary scan test is used to test

(a) Pins (b) Multipliers (c) Boards (d) wires

8. CMOS domino logic occupies

(a) Smaller area (b) Larger area
(c) Both of the mentioned (d) None of the mentioned

9. Test Benches procedure is _____

(a) Smaller design (b) Larger design
(c) Complicated (d) None of the mentioned

10. Blocking & Non blocking assignment is

(a) =statement & ≤ statement (b) ≤ statement
(c) Statement (d) ≥ statement & =statement

PART - B (5 x 2 = 10 Marks)

11. What is Body effect and channel Length modulation?

12. Define design margin.

13. Draw the pseudo nmos inverter.

14. What is stuck – at fault?

15. What is the structural gate-level modeling?

PART - C (5 x 16 = 80 Marks)

16. (a) Explain layout design rules in detail. (16)

Or

(b) (i) Explain the DC transfer characteristics of CMOS inverter with necessary conditions for the different regions. (8)

(ii) Obtain the threshold voltage equation for different threshold voltage effects. (8)

17.(a) Explain the concept of delay estimation, logical effort and sizing of MOSFET. (16)

Or

(b) Explain the static and dynamic power dissipation in CMOS circuits with necessary diagrams and expressions. (16)

18. (a) Explain in detail: (i) Conventional CMOS Latch (ii) Conventional CMOS Flip flop. (16)

Or

(b) Explain in detail about sequencing dynamic circuits and synchronizers. (16)

19. (a) Explain system level test techniques/boundary scan test. (16)

Or

(b) (i) Explain Ad-Hoc testing and Built in soft test techniques. (8)

(ii) What are the challenges involved in silicon debugging? Explain. (8)

20. (a) Explain the concept involved in structural gate level modeling and also give the description for Decoder and parity encoder. (16)

Or

(b) Write the verilog code in gate level modeling for multiplexer and D-latch. (16)

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