Reg. No. : | | | | | | | | | | |

Question Paper Code: 36404

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2018

Sixth Semester

Electronics and Communication Engineering

01UEC604 - VLSI DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. Define body effect.
2. Give the types of design rules.
3. State the types of power dissipation.
4. State the types of power dissipation.
5. Differentiate latch and flip-flop.
6. State any two criteria for low power logic design.
7. What is the need for testing?
8. What is mean by logic verification?
9. Mention the possible values which are allowed in Verilog HDL.
10. What are gate primitives?

PART - B (5 x 16 = 80 Marks)

11. (a) Explain in detail about ideal I-V characteristics and non-ideal characteristics of MOSFET. (16)

Or

(b) Illustrate the DC transfer characteristics of a CMOS inverter. (16)

12. (a) What is Power Dissipation? Explain the various ways to minimize the static and dynamic power dissipation. (16)

Or

(b) Demonstrate the concept of device characterization in CMOS processes. (16)

13. (a) Compare the various logic circuit families. (16)

Or

(b) (i) Discuss about the conventional CMOS flip flops. (8)

(ii) Summarize the sequencing of dynamic circuits. (8)

14. (a) Discuss about logic verification in detail. (16)

Or

(b) Explain the method of boundary scan test in detail. (16)

15. (a) (i) Develop a Verilog code for 4 – bit comparator using behavioral modeling. (8)

(ii) Develop a Verilog code for 2 – bit multiplexer using gate level modeling. (8)

Or

(b) Explain behavioral and gate level modeling with suitable example. (16)