Reg. No. : | | | | | | | | | | |

Question Paper Code: 43506

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2018

Third Semester

Electronics and Instrumentation Engineering

14UEI306 – DIGITAL ELECTRONICS

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. The three basic logic gates are

   (a) AND,OR and NOT gate (b) AND,OR and NOR
   (c) NAND, OR and NOT (d) None of the above

2. _____ gates are called as the universal gates

   (a) AND and OR (b) NAND and NOR
   (c) NOT and NOT (d) NAND and OR

3. The systematic reduction of logic circuits is accomplished by

   (a) Using Boolean algebra (b) Symbolic reduction
   (c) TTL logic (d) Using a truth table

4. A comparator is a special combinational circuit designed primarily to compare the relative magnitude of _____ numbers .

   (a) two decimal (b) three decimal (c) two binary (d) three binary

5. D flip-flop during the occurrence of clock pulse if ____, the output ____ and if _____, the output is reset.

(a) D = 0, Q = 0 , D is set (b) D = 1, Q = 1 , D = 0

(c) D = 1, Q is set , D = 0 (d) None of the above

6. What is a major disadvantage of RAM?

(a) Its access speed is too slow (b) Its matrix size is too big

(c) It is volatile (d) High power consumption

7. In positive logic, _____

(a) a HIGH = 1, a LOW = 0 (b) a LOW = 1, a HIGH = 0

(c) only HIGHs are present (d) only LOWs are present

8. For JK flip flop with J=1, K=0, the output after clock pulse will be _____

(a) 0 (b) 1 (c) High Impedance (d) No change

9. PAL consists of a programmable ____ array and a fixed _____ array with output logic.

(a) NAND and NOR (b) AND and NOR

(c) NAND and OR (d) AND and OR

10. _____ is the minimum time required to maintain a constant voltage levels at the excitation inputs of the flip-flop device.

(a) Rise time (b) Fall time

(c) Setup time (d) None of these

PART - B (5 x 2 = 10 Marks)

11. Simplify: $A + AB + \overline{A} + B$.

12. Write the truth table of a 4:1 multiplexer.

13. Define synchronous counter.

14. Define Glitch.

15. What is meant by PLA?

PART - C (5 x 16 = 80 Marks)

16. (a) (i) Give a brief note on Weighted codes. (8)

(ii) If $\bar{A}B + C\bar{D} = 0$ then. Prove that $AB + \bar{C}(\bar{A} + \bar{D}) = AB + BD + \bar{B}\bar{D} + \bar{A}\bar{C}D$. (8)

Or

(b) Simplify the Boolean function using tabulation method.
Y (A, B, C, D)= ∑ m (1, 2, 3, 5, 9, 12, 14, 15)+∑ D (4, 8, 11). (16)

17. (a) (i) Implement $F = (A\bar{B} + \bar{A}B)(C + \bar{D})$ using only NOR gates. (10)

(ii) Implement a Half adder. (6)

Or

(b) (i) Discuss the 4-bit Magnitude comparator with its logic diagram. (8)

(ii) Write the truth table of a three - to - eight lines decoder and construct the circuit for 3 - to - 8 lines decoder. (8)

18. (a) (i) How will you convert a D flip flop into JK flip flop? (8)

(ii) Sketch a 4-bit serial in serial out shift register and draw its waveforms. (8)

Or

(b) Explain the operation universal shift register with logic diagram. (16)

19. (a) Design an Asynchronous circuit that has two inputs x_1 and x_2 and output z. The circuit is required to give an output whenever the input sequence (0,0) (0,1) and (1,1) received but only in that order. (16)

Or

(b) What is a hazard? Explain the different types of hazards. Discuss in detail how hazards can be eliminated. (16)

20. (a) Explain about RAM and its types. (16)

Or

(b) (i) With a neat sketch, explain the block diagram of PLA. (8)

(ii) Discuss in detail about EPROM and EEPROM. (8)

43506