**Reg. No. :** | | | | | | | | | | |

# Question Paper Code: 47504

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2018

Seventh Semester

Electronics and Instrumentation Engineering

14UEI704 - VLSI SYSTEM DESIGN

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. nMOS devices are formed in

   (a) p-type substrate of high doping level

   (b) n-type substrate of low doping level

   (c) p-type substrate of moderate doping level

   (d) n-type substrate of high doping level

2. Source and drain in nMOS device are isolated by

   (a) A single diode (b) Two diodes (c) Three diodes (d) Four diodes

3. If n-transistor conducts and has large voltage between source and drain, then it is said to be in _____ region

   (a) Linear (b) Saturation (c) Non saturation (d) Non saturation

4. In Rise time , the time needed for the output voltage to rise from

   (a) 0.9 $V_{dd}$ to 0.1 $V_{dd}$ (b) 0.1$V_{dd}$ to 0.9 $V_{dd}$

   (c) 0.09 $V_{dd}$ to 0.1 $V_{dd}$ (d) 0.01Vddto0.9 Vdd

5. In dynamic CMOS logic _____ is used

(a) Two phase clock (b) Three phase clock
(c) One phase clock (d) Four phase clock

6. Which multiplier is very well suited for twos complement numebers?

(a) Baugh-wooley algorithm (b) Wallace trees
(c) Dadda multipliers (d) Modified booth encoding

7. PAL has

(a) Programmable AND array and a fixed OR array
(b) Programmable OR array and a fixed AND array
(c) Programmable AND and OR array
(d) All the above

8. Which type of device FPGA are?

(a) SLD (b) SROM (c) EPROM (d) PLD back

9. What do VHDL stand for?

(a) Verilog hardware description language (b) VHSIC hardware description language
(c) very hardware description language (d) VMEbus description language

10. Among the VHDL features ,which language statements are executed at the same time in parallel flow

(a) concurrent (b) sequentia (c) net-list (d) test bench

PART - B (5 x 2 = 10 Marks)

11. Draw the transistor circuit symbol of nMOS depletion mode

12. What is stick diagram? What are the uses of stick diagram?

13. Draw the nMOS switch logic implementation of four –way multiplexer

14. What is programmable logic array?

15. Give the classification of operators used in VHDL.

PART - C (5 x 16 = 80 Marks)

16. (a) Explain in detail about MOS transistor with the working operation of enhancement mode and depletion mode (16)

Or

(b) Explain in detail about the scaling concept of MOS Transistor (16)

17. (a) Describe the base operation of nMOS inverter. Also determine the pull-up to pull down ratio for an nMOS inverter driven through one or more pass transistors. (16)

Or

(b) Explain in detail about the Stick Diagram and layout diagram. (16)

18.(a) Discuss in detail about the Dynamic CMOS design. (16)

Or

(b) Design a $2^s$ complement multiplication using Baugh Wooley method. (16)

19. (a) Write short notes on floor planning, placement and routing of FPGA. Also explain with a neat FPGA architecture. (16)

Or

(b) Explain in detail about Floor planning, Routing &Placement. (16)

20. (a) Write VHDL testbench code for 4:1 multiplexer. (16)

Or

(b) Write a VHDL behavioral coding of MOD-7 counter. (16)