Reg. No. : | | | | | | | | | | |

Question Paper Code: 43203

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2018

Third Semester

Computer Science and Engineering

14UCS303 - COMPUTER ORGANIZATION AND ARCHITECTURE

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

(Smith chart may be permitted)

PART A - (10 x 1 = 10 Marks)

1. Which of the following would take less execution time?

   (a) Memory –Memory instruction (b) Register – Register instruction
   (c) Register – memory instruction (d) Memory – register instruction

2. Add 20(R0,R1) , R2 is an example of

   (a) Indirect addressing (b) Absolute addressing
   (c) Indexed Addressing (d) Direct Addressing

3. How many full adders are required for *k* bit addition?

   (a) *k* (b) *k*+1 (c) 2*k* (d) *k*-1

4. In IEEE 32-bit representations, the mantissa of the fraction is said to occupy _____ bits.

   (a) 24 (b) 23 (c) 20 (d) 16

5. The throughput of an ideal pipeline with *k* stages is _____ instruction/clock cycle

   (a) *k* (b) *k*-1 (c) 1 (d) 2

6. If an exception is raised and the succeeding instructions are executed completely, then the processor is said to have

(a) Exception handling (b) Imprecise exceptions
(c) Error correction (d) None of these

7. The cost of parallel processing is primarily determined by

(a) Time complexity (b) Switching complexity
(c) Circuit complexity (d) None of the above

8. In a multithreaded environment _____

(a) Each thread is allocated with new memory from main memory
(b) Main thread terminates after the termination of child threads
(c) Every process can have only one thread
(d) No termination

9. The extra time needed to bring the data into memory in case of a miss is called as _____

(a) Delay (b) Propagation time (c) Miss penalty (d) Data latency

10. Which interrupt is un-maskable?

(a) RST 5.5 (b) RST 7.5 (c) TRAP (d) Both a and b

PART - B (5 x 2 = 10 Marks)

11. Why the data bus is bidirectional while the address bus is unidirectional?

12. What is the purpose of guard bits in floating point operations?

13. How do you handle the data hazard?

14. Define interleaved or fine grained multithreading.

15. What is polling?

PART - C (5 x 16 = 80 Marks)

16. (a) (i) With a neat diagram, explain the basic operational steps needed to execute the instruction Add LOCA, R0. (8)

(ii) How would you measure and report the performance of a computer? (8)

Or

(b) (i) Describe the different classes of Instruction format with examples. (12)

(ii) Registers *R*1 and *R*2 of a computer contain the decimal values 1200 and 2400 respectively. What is the effective address of the memory operand in each of the following instructions?

Load 20(*R*1), *R*5

Add –(*R*2), *R*5 (4)

17. (a) (i) Design a fast adder by deriving generate and propagate functions. (8)

(ii) Explain the steps in Booth algorithm. (8)

Or

(b) Derive and explain an algorithm for adding and subtracting two floating point binary numbers. (16)

18. (a) Explain the super scalar operations with a neat diagram. (16)

Or

(b) Discuss the various hazards that might arise in a pipeline. What are the remedies commonly adopted to overcome / minimize these hazards? (16)

19. (a) Explain Flynn's classification of computers. (16)

Or

(b) Discuss in detail instruction level parallelism. (16)

20. (a) What is virtual memory? Explain the address translation scheme. (16)

Or

(b) (i) What is DMA? What are the steps in DMA transfer? (8)

(ii) Explain the working of a DMA controller with a diagram. (8)

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