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Question Paper Code: 33203

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2018

Third Semester

Computer Science and Engineering

01UCS303 - COMPUTER ORGANIZATION AND ARCHITECTURE

(Regulation 2013)

Duration: Three hours

Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. State the basic functional units of a computer.
2. What do you mean by stored program concept?
3. What is Subword Parallelism?
4. List the features of booth multiplication algorithm.
5. What is meant by Data path?
6. Define branch folding.
7. Give an example for WAW Hazard.
8. What is instruction level parallelism?
9. Define TLB hit and Miss.
10. What is meant by bus arbitration?

PART - B (5 x 16 = 80 Marks)

11. (a) (i) Explain the basic functional units of a computer with a diagram. (8)
(ii) With a neat diagram, explain the basic operational steps needed to execute the instruction *ADD R2, (R2)*. (8)

Or

(b) Write in detail about various addressing modes. (16)

12. (a) (i) What are the advantages of using carry look ahead adder? (4)

(ii) Discuss the booth's multiplication algorithm. Illustrate with the example $25 * (-16)$. (12)

Or

(b) Explain the floating point addition steps and algorithm in detail. (16)

13. (a) Explain how a data path would be modified for pipelined execution. Illustrate with the help of a neat block diagram. (16)

Or

(b) Discuss the various hazards that might arise in a pipeline. What are the remedies commonly adopted to overcome/minimize these hazards. (16)

14. (a) Explain the Multiple-instruction multiple-data streams (MIMD) parallel architecture functions with suitable block diagram. (16)

Or

(b) Explain how performance efficiency is achieved by Multicore Processors. (16)

15. (a) What are the types of implementation in virtual memory? Explain in detail the address translation mechanism of each of them. (16)

Or

(b) How does a virtual address get translated into physical address? Explain in detail with the neat diagram. Explain the use of TLB. (16)
