Reg. No. : | | | | | | | | | | |

Question Paper Code: 52738

M.E. DEGREE EXAMINATION, NOV 2016

Elective

VLSI Design

15PVL508 - TESTING OF VLSI CIRCUITS

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

(5 x 20 = 100 Marks)

1. (a) Discuss in detail about delay models. (20)

Or

(b) Explain fault dominance in combinational and sequential circuit. (20)

2. (a) Explain D algorithm with an example. (20)

Or

(b) Explain FAN algorithm with an example. (20)

3. (a) Discuss in brief about system level DFT. (20)

Or

(b) What are the rules for LSSD design and LSSD double latch design? (20)

4. (a) Explain various test algorithms for RAM. (20)

Or

(b) Explain various types of BIST architecture. (20)

5. (a) Describe in detail Self-checking in combinational and sequential circuits. (20)

Or

(b) Explain the technique of diagnosis by UUT reduction in detail. (20)

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