Reg. No. : | | | | | | | | | | |

Question Paper Code: 41632

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2016

Third Semester

Instrumentation and Control Engineering

14UIC302 – DIGITAL LOGIC CIRCUITS AND DESIGN

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 1 = 10 Marks)

1. The Hexadecimal equivalent of a decimal number 48 is

   (a) 2B (b) 2E (c) 2F (d) F2

2. What are the symbols used to represent digits in the binary number system?

   (a) 0,1 (b) 0,1,2 (c) 0 through 8 (d) 1,2

3. What is ROM?

   (a) repeat on memory
   (b) read on memory
   (c) read only memory
   (d) repeat only memory

4. In PROM, we can

   (a) store the data once and read multiple times
   (b) store and erase data once
   (c) store and erase data multiple times
   (d) store once and read once

5. Select the correct characteristic equation of a SR flipflop.

   (a) $Qn + 1 = \overline{S} + RQn$
   (b) $Qn + 1 = S + \overline{R}\,Qn$
   (c) $Qn + 1 = S + RQn$
   (d) none of the above

6. Which type of gate can be used to add two bits?

(a) Ex-OR (b) Ex-NOR (c) Ex-NAND (d) NOR

7. The next state variables in asynchronous sequential circuits are called

(a) secondary variables (b) excitation variables
(c) primary variables (d) short term memory

8. In ASM, the decision box is represented by

(a) circle (b) oval (c) diamond (d) rectangle

9. Which of the following logic family has the shortest propagation delay?

(a) CMOS (b) NMOS (c) ECL (d) 74Sxx

10. The VHDL is based on the _____ library

(a) IEE (b) WORK (c) IEEE (d) Standard

PART - B (5 x 2 = 10 Marks)

11. State Demorgan's Theorem.

12. Define fan in and fan out.

13. Compare combinational and sequential circuits

14. What is race around condition?

15. List the configuration of TTL.

PART - C (5 x 16 = 80 Marks)

16. (a) Reduce the following functions using K-map techniques.

(i) $f(A, B, C, D) = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$ (8)
(ii) $f(A, B, C, D) = \prod M(0, 3, 4, 7, 8, 10, 12, 14) + d(2, 6)$ (8)

Or

(b) (i) Design a 2 bit magnitude comparator. (8)

(ii) Explain the operation of 4 to 10 decoder. (8)

17. (a) Design and draw 4 bit binary to gray code converter and explain. (16)

Or

(b) (i) Explain in detail about PLA with a specific example. (8)

(ii) Explain with neat diagrams RAM architecture. (8)

18. (a) (i) Realize a SR flip flop using NAND gates and explain its operation. (8)

(ii) Design a 3-bit binary up-down counter (8)

Or

(b) Design a four state down counter using T flip flop. (16)

19. (a) Draw the fundamental mode asynchronous circuit and explain in detail. (16)

Or

(b) (i) What is the procedure for obtaining the transition table form the circuit diagram of an asynchronous sequential circuit? (8)

(ii) Discuss in detail the race conditions. (8)

20. (a) Explain the various modeling methods used in VHDL with an example. (16)

Or

(b) (i) Write VHDL code for a full sub tractor using logic Equation. (8)

(ii) Write a VHDL description of an S-R latch using a process. (8)

———————