Reg. No. : | | | | | | | | | | |

Question Paper Code: 51336

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2016

Third Semester

Electrical and Electronics Engineering

15UEE306 - DIGITAL LOGIC CIRCUITS

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. In standard TTL the 'totem pole' stage refers to the

   (a) multi-emitter input stage (b) phase splitter
   (c) output buffer (d) open collector output stage

2. What is the gray code for 1000?

   (a) 1010 (b) 1000 (c) 1011 (d) 1100

3. The digital multiplexer is basically a combination logic circuit to perform the operation of

   (a) AND-AND (b) OR-OR (c) AND-OR (d) OR-AND

4. A combinational circuit that performs the addition of two bits is called

   (a) Full adder (b) Full subtractor (c) Half subtractor (d) Half adder

5. The output Q_n of a J-K flip-flop is zero. It change to one when a clock pulse is applied. The input J_n and K_n are respectively

   (a) 1 and X (b) 0 and X (c) X and 0 (d) X and 1

6. A flip-flop output transition serves as clock to next flip-flop is called

(a) ripple counter (b) parallel counter
(c) shift register (d) none of the above

7. An unwanted switching transients occurs at the output of a circuit are

(a) races (b) cycles (c) hazards (d) harmonics

8. A PLA can be used

(a) as a microprocessor (b) as a dynamic memory
(c) to realize a sequential logic (d) to realize a combinational logic

9. Which one is unary operator in VHDL?

(a) +(sign) (b) not (c) mod (d) rol

10. Which is used to verify the design function?

(a) packages (b) libraries (c) test bench (d) subprogram

PART - B (5 x 2 = 10 Marks)

11. Define fan-in and fan-out.

12. Give the application of demultiplexer.

13. Distinguish between synchronous sequential circuits and asynchronous sequential circuit.

14. Define race in asynchronous sequential circuit.

15. What is test bench in VHDL.

PART - C (5 x 16 = 80 Marks)

16. (a) (i) Write a brief notes about error detection and correction codes. (8)

(ii) Explain the operation and characteristics of DTL circuit. (8)

Or

(b) (i) Explain the operation of TTL with neat circuit diagram for 2 input NAND gate with Tottem pole output. (12)

(ii) Write short notes on CMOS NOR gate. (4)

17. (a) Reduce the following using K-map

(i) $F(w, x, y, z) = \Sigma m(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$ (4)

(ii) $g(w, x, y, z) = \Sigma m(1, 3, 4, 6, 11) + \Sigma d(0, 8, 10, 12, 13)$ (4)

(iii) $Y = (A, B, C, D) = \prod M(0, 2, 8, 9, 12, 13, 15)$ (4)

(iv) $Y = (A, B, C, D) = \prod M(1, 2, 3, 8, 9, 10, 11, 14) + d(7, 15)$. (4)

Or

(b) (i) Implement Excess 3 to BCD code converter circuit. (8)

(ii) Implement the given boolean function using 4:1 Multiplexer,

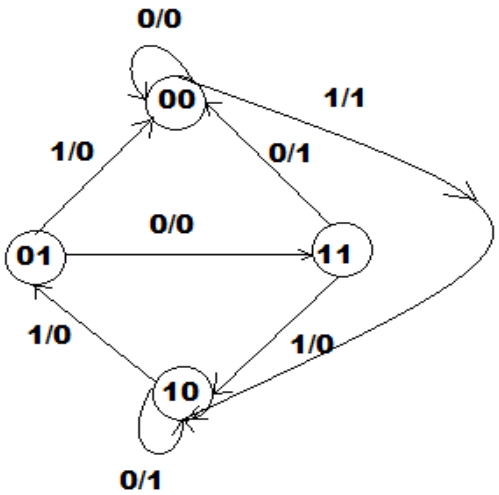
$F(A, B, C, D) = \sum m(0, 1, 2, 4, 6, 9, 12, 14)$. (8)

18. (a) (i) Design a 4-bit synchronous up-counter using JK flip flop. (8)

(ii) Using D-flip flop, design a synchronous counter which counts in the sequence 000, 001, 010, 011, 100, 101, 110, 111, 000. (8)

Or

(b) Design a sequential circuit with JK flip-flop. (16)



19. (a) Discuss the different types of hazards that occurs in asynchronous sequential circuits and combinational circuits. (16)

Or

(b) Explain with a suitable example the procedure for analyzing synchronous sequential circuit. (16)

20. (a) (i) Write a VHDL code for a full adder. (8)

(ii) Explain the operation of RTL data path design with suitable diagram. (8)

Or

(b) Write a VHDL code for SR flip flop and D flip flop. (16)
