Reg. No. : | | | | | | | | | | |

Question Paper Code: 52532

M.E. DEGREE EXAMINATION, NOV 2016

Third Semester

Power Electronics and Drives

15PPE302 – DIGITAL CONTROLLERS IN POWER ELECTRONICS APPLICATION

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (5 x 1 = 5 Marks)

1. How many indirect memory addressing options are possible in C2xx series

   (a) 6 (b) 5 (c) 4 (d) infinity

2. External interrupts (XINT1,XINT2) are controlled by

   (a) XINT1CR (b) XINT2CR
   (c) XINT1CR & XINT2CR (d) None of these

3. The resolution of ADC is

   (a) 10 (b) 16 (c) 8 (d) 2

4. CPLD is designed using

   (a) EEPROM (b) EPROM (c) ROM (d) RAM

5. A controlled rectifier with a DC shunt motor as a load is driving a shaft connected to a conveyer belt, what happens, when the duty ratio of the rectifier is increased

   (a) Speed increase (b) speed decreases
   (c) Increases initially then gradually decreases (d) No change

PART B - (5 x 3 = 15 Marks)

6. Write some of the advanced features of LF2407.

7. Draw the block diagram of multiplexing of a single pin.

8. List the trigger sources for DSP controller ADC.

9. What are the types of FPGA?

10. Write the structure of VHDL Programming.

PART C - (5 x 16 = 80 Marks)

11. (a) (i) Explain the various memory addressing modes of TMS320LF2407 DSP processor. (10)

(ii) Draw the general architecture of 240XA devices. (6)

Or

(b) Explain about graphical overview of DSP core and peripherals on the LF2407 in detail. (16)

12. (a) With a neat block diagram, explain about the Peripherals Interrupt Expansion (PIE) controller. (16)

Or

(b) Explain the different hierarchical level and how an interrupt request signal propagates through them. (16)

13. (a) Describe the operation of the analog to digital converter of the DSP processor. (16)

Or

(b) Draw and explain the basic functional blocks of event manager with necessary diagram. (16)

14. (a) Describe with necessary diagrams about the Configurable Logic Blocks (CLB) and Programmable Interconnect Point (PIP) of FPGA processor. (16)

Or

(b) Sketch and explain the block diagram of Xup Virtex –II Pro FPGA development system and write its board components. (16)

15. (a) Explain the application of FPGA control in PWM controlled induction motor as a case study. (16)

Or

(b) Design a VHDL program for a PWM inverter and formulate the digital firing control logic to get a desired output AC voltage. (16)