Reg. No. : | | | | | | | | | | |

Question Paper Code: 41336

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2016

Third Semester

Electrical and ElectronicsEngineering

14UEE306 - DIGITAL LOGIC CIRCUITS

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. Convert $(10111.10)_2$ to decimal equivalent

   (a) $(23.5)_{10}$ (b) $(46.5)_{10}$ (c) $(23.2)_{10}$ (d) $(46.2)_{10}$

2. What is the major advantage of ECL logic?

   (a) very high speed (b) wide range of operating voltage
   (c) very low cost (d) very high power

3. The output of an exclusive-NOR gate is 1. Which input combination is correct?

   (a) A=1, B=0 (b)A=0, B=1 (c) A=0, B=0 (d) none of these

4. To implement the expression $A\overline{B}CD + AB\overline{C}D + ABC\overline{D}$, it takes one OR gate and

   (a) three AND gates and three inverters (b) three AND gates and four inverters
   (c) three AND gates (d) one AND gate

5. When a flip-flop is set, its output will be?

   (a) $Q = 1, \overline{Q} = 0$ (b) $Q = 0, \overline{Q} = 1$ (c) $Q = 0, \overline{Q} = 0$ (d) $Q = 1, \overline{Q} = 1$

6. In the toggle mode a JK flip-flop has

   (a) J = 0, K = 0 (b) J = 1, K = 1 (c) J = 0, K = 1 (d) J = 1, K = 0

7. Which of the statement is true about static-1 hazard?

(a) output goes momentarily goes to 0 when it should remain at 1
(b) output goes momentarily goes to 1 when it should remain at 0
(c) output changes 3 or more times
(d) none of these

8. What programmable technology is used in FPGA devices?

(a) SRAM (b) FLASH (c) Antifuse (d) All the above

9. How are the statements between BEGIN and END not evaluated in VHDL?

(a) Constantly (b) Simultaneously
(c) Concurrently (d) Sequentially

10. How many styles of modeling are there in VHDL?

(a) 2 (b) 4 (c) 3 (d) 1

PART - B (5 x 2 = 10 Marks)

11. Define fan-in and fan-out.

12. Why is MUX called as data selector?

13. Convert a D flip-flop into T flip-flop.

14. What is PLA?

15. Write VHDL code for half adder.

PART - C (5 x 16 = 80 Marks)

16. (a) (i) Convert the following

(a) $(764.352)_8$ to hexadecimal

(b) $(7A4.BA)_H$ to binary (8)

(ii) Explain Gray code and Binary code. (8)

Or

(b) (i) Explain the working of two input TTL NAND totem pole output gate. (8)

(ii) Explain the working of two input CMOS NAND gate. (8)

17. (a) Minimize and implement the following Boolean expression

(i) $F(A,B,C,D) = \sum m\,(1,3,5,8,9,11,15) + \sum d\,(2,13)$ (8)

(ii) $F(A,B,C,D) = \Pi M\,(1,2,3,8,9,10,11,14) + \sum d\,(7,15)$. (8)

Or

(b) (i) Design a logic circuit to convert the Binary to Gray code. (8)

(ii) Implement a full subtractors using half subtractors. (8)

18. (a) Design a synchronous counter using JK FF to count following sequence: 7, 6, 5, 4, 3, 2, 7. (16)

Or

(b) (i) Explain about 4-bit ripple up counter. (8)

(ii) Discuss the function of a universal shift register. (8)

19. (a) Describe the steps involved in design of asynchronous sequential circuit in detail with an example. (16)

Or

(b) (i) An asynchronous sequential circuit is described by the following excitation and output function.

$Y=x_1\ x_2'+(x_1 + x_2')y$

$Z=y$

(1) Draw the logical diagram of the circuit

(2) Derive the transition table and output map.

(3) Obtain flow table. (8)

(ii) Implement the following function using $PLAF_1 = \sum m\ (4, 5, 7)$ and $F_2 = \sum m\ (3, 5, 7)$. (8)

20. (a) Write VHDL program for 4-bit ripple carry adder using structural modeling. (16)

Or

(b) Write a VHDL program and explain the design procedure of 4-bit comparator. (16)

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