Reg. No. : | | | | | | | | | | |

Question Paper Code: 41432

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2016

Third Semester

Electronics and Communication Engineering

14UEC302 – DIGITAL ELECTRONICS AND DESIGN

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. The equivalent hexadecimal of binary number 1011101.1011 is

   (a) B33 (b) EFF2.F (c) 5 D.B (d) 4A.67

2. The simplified logic of the Boolean function $x'y'z + x'yz + xy'$ is

   (a) $x'yz+xyz$ (b) $x'z + xy'$ (c) $x'z'+ x'y'$ (d) $xz+xy$

3. The logic required to decode the binary $(1011)_2$ by producing a HIGH indication on the output Y is

   (a) $Y = \bar{D}C\,\bar{B}\bar{A}$ (b) $Y= D\bar{C}\,BA$ (c) DC BA (d) $\bar{D}\bar{C}\,\bar{B}\bar{A}$

4. The circuit that generates the parity bit in the transmitter is

   (a) Parity checker (b) Parity generator

   (c) Both (a) and (b) (d) None of these

5. How many flip flops are required to construct a mod 128 counter

   (a) 4 (b) 3 (c) 7 (d) 5

6. How many flip-flops are required to design mod-6 counter?

   (a) 4 (b) 6 (c) 3 (d) 8

7. CMOS fan out depends on

(a) power dissipation (b) propagation delay

(c) current (d) noise margin

8. The PLD with programmable AND array and fixed OR array is

(a) PAL (b) PLA (c) PROM (d) CPLD

9. A circuit which do not operate in synchronous with clock signal is

(a) Synchronous sequential circuits (b) Asynchronous sequential circuits

(c) FPGA (d) combinational circuits

10. In this mode the inputs and outputs are represented by levels

(a) Fundamental mode (b) Pulse mode

(c) Both (a) and (b) (d) None of these

PART - B (5 x 2 = 10 Marks)

11. Obtain the canonical sum of product form of the function: $Y=AB + ACD$.

12. Draw the 4-bit binary divider.

13. Write the excitation table of RS flip-flop.

14. How does a static RAM differ from dynamic RAM?

15. Give the general model of ASM?

PART - C (5 x 16 = 80 Marks)

16. (a) Simplify the following expression using Quine Mccluskey method
$f [w, x, y , z] = \sum (0, 2, 3, 5, 6, 7, 8, 9) + d (10, 11, 12, 13, 14, 15)$
Realize the minimized function using NOR gates only. (16)

Or

(b) (i) Simplify the Boolean function using K-map

$F (w, x, y, z) = \Sigma (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$. (8)

(ii) Implement the following function with NAND gate only

$F (x, y, z) = \Sigma (0, 6)$. (8)

17. (a) (i) With logic diagram Truth table and explain about 3-to-8 decoder. (6)

(ii) Define multiplexer and implement the Boolean function with a suitable multiplexer. $F(A, B, C, D) = \Sigma(0, 1, 3, 4, 8, 9, 15)$. (10)

Or

(b) With Truth table, design BCD-to-excess-3 code converter and obtain its logic diagram. (16)

18. (a) Explain synchronous decade counter using T flip flop. (16)

Or

(b) (i) Realize D flip-flop using SR flip-flop. (8)

(ii) With neat illustration explain in detail about 4-bit parallel-in-serial out shift register. (8)

19. (a) With block diagram explain about PLA and realize the following functions in PLA:

$$F1 = \overline{A}\ B\ \overline{C} + A\ \overline{B}\ C + \overline{A}\ B\ C$$

$$F2 = A\ B + A\ C + \overline{A}BC$$

(16)

Or

(b) (i) Differentiate registered PAL and configurable PAL (8)

(ii) Design a 4-bit binary–to gray code converter using PROM. (8)

20. (a) (i) Develop VHDL code for 3 to 8 decoder. (8)

(ii) Explain the method to eliminate static hazard in an asynchronous circuit with an example. (8)

Or

(b) Design an asynchronous sequential circuit that has two inputs x_1 and x_2 and one output z. The output z = 1 if x_1 changes from 0 to 1, z = 0 if x_2 changes from 0 to 1 and z = 0 otherwise. Realize the circuit using D FF. (16)

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