Reg. No. : | | | | | | | | | | |

Question Paper Code: 31464

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2016

Sixth Semester

Electronics and Communication Engineering

01UEC604 - VLSI DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. What is channel length modulation?
2. What is meant by interconnect? What the types are of interconnect?
3. How to compute the delay of CMOS circuits?
4. What is the fundamental goal in device modeling?
5. What is meant by transparent latch? Draw any two types of transparent latch and write its limitation.
6. What is meant by synchronizer?
7. What is the need for testing?
8. What is boundary scan?
9. Give the basic difference between tasks and functions.
10. What are bitwise operators in Verilog?

PART - B (5 x 16 = 80 Marks)

11. (a) Explain in detail about ideal I-V characteristics and non-ideal characteristics of MOSFET. (16)

Or

(b) Explain the DC characteristic of CMOS inverter. (16)

12. (a) (i) Explain the static and dynamic power dissipation in CMOS circuit with necessary diagram and expression. (10)

(ii) Give a brief account on design margin. (6)

Or

(b) (i) Explain the interconnect delay modeling. (8)

(ii) Explain about various level of device models in MOSFET. (8)

13. (a) (i) Explain the issues related to the design of low power logic design. (8)

(ii) In short explain about static CMOS design. (8)

Or

(b) (i) Write short notes on pulsed latch. (8)

(ii) Explain the concept of synchronizer. (8)

14. (a) Explain in detail about boundary scan test. (16)

Or

(b) (i) What is the need of testing? Explain the types of testing. (8)

(ii) In short explain about logic verification principles. (8)

15. (a) Write a Verilog HDL code for

(i) 2:4 decoder (ii) Equality detector using gate level modelling. (16)

Or

(b) (i) Explain blocking procedural assignment and non-blocking assignment. (8)

(ii) Write a behavioural level verilog HDL program for 1x8 multiplexer circuit. (8)

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