Reg. No. : | | | | | | | | | | |

Question Paper Code: 31467

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2016

Elective

Electronics and Communication Engineering

01UEC903 - COMPUTER ARCHITECTURE AND ORGANIZATION

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. What is big-endian and little–endian arrangement?. Give examples.
2. Differentiate Von-Neumann and Harvard architecture.
3. Write the advantages of carry save and carry look-ahead adder.
4. Define underflow.
5. Give the important features of bit slicing.
6. Specify the design considerations for micro-programmed sequencing.
7. Compare sequential access and random access memories.
8. State the principles of memory interleaving.
9. Mention the significance of buses and its types in computer architecture.
10. Highlight the need for handshaking in I/O design.

PART - B (5 x 16 = 80 Marks)

11. (a) (i) Describe the evolution of computers. (8)

(ii) Explain the instruction types designed for computers. (8)

Or

(b) (i) Discuss the design aspects of computer architecture at register level. (10)

(ii) Why different addressing modes are used in computers? Write the merits and demerits of different addressing modes. (6)

12. (a) (i) With example illustrate the principle and working of binary multiplication used in computers. (8)

(ii) Write the significance and basic idea of pipeline processing. (8)

Or

(b) (i) Describe the algorithm used for non-restoring division of binary numbers. (10)

(ii) Write the importance of co-processor for floating point operations. (6)

13. (a) (i) Explain the various issues in data path implementation. (10)

(ii) Compare horizontal and vertical organization of architecture design. (6)

Or

(b) (i) Describe the design details of pipelined processing. (10)

(ii) Write short notes on Nano programming. (6)

14. (a) (i) Describe the construction and working of different types of ROM. (8)

(ii) Explain the concepts of virtual memory. (8)

Or

(b) (i) Explain the direct mapping procedure for organization of cache memory. (8)

(ii) Write the principle of magnetic surface recording. (8)

15. (a) (i) Discuss the details of bus interfacing in system organization. (10)

(ii) Write short notes on vector processor. (6)

Or

(b) (i) Explain the design aspects of vectored interrupts. (10)

(ii) Compare CISC and RISC processors. (6)
