Reg. No. : | | | | | | | | | | |

Question Paper Code: 51534

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2016

Third Semester

Electronics and Instrumentation Engineering

15UEI304 - DIGITAL ELECTRONICS

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. Which of the following is minimum error code?

   (a) Octal code (b) Grey code
   (c) Binary code (d) Excess 3 code

2. Which of the following expressions is in the sum-of-products (SOP) form?

   (a) $AB + CD$ (b) $AB(CD)$ (c) $(A + B)(C + D)$ (d) $(A)B(CD)$

3. A NAND gate is called a universal logic element because

   (a) it is used by everybody
   (b) any logic function can be realized by NAND gates alone
   (c) all the minization techniques are applicable for optimum NAND gate realization
   (d) many digital computers use NAND gates

4. The number of full and half-adders required to add 16-bit numbers is

   (a) 8 half-adders, 8 full-adders (b) 1 half-adder, 15 full-adders
   (c) 16 half-adders, 0 full-adders (d) 4 half-adders, 12 full-adders

5. For which of the following flip-flops, the output is clearly defined for all combinations of two inputs

   (a) Q type flip-flop (b) R-S flip-lop (c) J-K flip-lop (d) D flip-flop

6. What is the difference between a ring shift counter and a Johnson shift counter?

   (a) there is no difference (b) a ring is faster
   (c) the feedback is reversed (d) the Johnson is faster

7. Which hazard is overcome by properly designed two level AND-OR or OR-AND circuit

   (a) dynamic hazard (b) static-0 hazard
   (c) static-1 hazard (d) none of the above

8. Which one is the suitable to detecting the hazard in circuit?

   (a) Logic gates (b) Karnaugh map
   (c) Boolean expression (d) None of these

9. Which of the following memories uses one transistor and one capacitor as basic memory unit

   (a) SRAM (b) DRAM (c) Both (a) and (b) (d) none

10. In a read-only memory information can be stored

    (a) at the time of fabrication
    (b) by the user only once during its life time
    (c) by the user a number of times
    (d) in any of the above ways depending upon the type of memory

PART - B (5 x 2 = 10 Marks)

11. Define De-morgan's theorem.

12. Draw $Y = A + BCD'$ using NAND only.

13. Write down the characteristic equation for JK flip flop.

14. Compare static and dynamic hazards.

15. Describe RAM and its block diagram.

PART - C (5 x 16 = 80 Marks)

16. (a) (i) Convert the binary number $(101111.1101)_2$ in to decimal. (4)

(ii) Convert the hexadecimal number in to decimal A3BH and 2F3H. (4)

(iii) Design a 4 bit BCD to Excess-3 code converter. (8)

Or

(b) Simplify the following expression using K-map

(i) $Y = \sum_m (7, 9, 10, 11, 12, 13, 14, 15)$

(ii) $Y = m_1 + m_5 + m_{10} + m_{11} + m_{12} + m_{13} + m_{15}$ (16)

17. (a) (i) Examine about the formation of inverter using CMOS and its operation. (8)

(ii) Identify the TTL logic circuit for a 3-input NAND gate with appropriate explanation. (8)

Or

(b) (i) Give the CMOS logic circuit for NOR gate and explain its operation. (8)

(ii) Explain the TTL circuit output connections. (8)

18. (a) (i) Explain the triggering of flip flops. (8)

(ii) Draw the logic diagram of master slave JK flip flop. (8)

Or

(b) Explain the operation of universal shift register with logic diagram. (16)

19. (a) (i) List out the steps involved in the design procedure of an asynchronous sequential circuit. (6)

(ii) When do you get the critical and non-critical race? How will you obtain race free conditions? (10)

Or

(b) What are hazards? When does the hazard occur in combinational circuits and quote an example? Name the types of hazards and how they are avoided. (16)

20. (a) Explain ROM, ROM architecture, types of ROM and its application. (16)

Or

(b) (i) Draw the block diagram of a PLA and explain its IC 7575-PLA. (16)
