Reg. No. :

Question Paper Code: 41536

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2016

Third Semester

Electronics and Instrumentation Engineering

14UEI306 – DIGITAL ELECTRONICS

(Regulation 2014)

Duration: Three hours   Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 1 = 10 Marks)

1. Find the hexadecimal equivalent of the octal number 153.4.

    (a) B6.8   (b) 68.8   (c) 6B.8   (d) 6B.6

2. _____ gates are called as the universal gates

    (a) AND and OR   (b) NAND and NOR
    (c) NOT and NOT   (d) NAND and OR

3. A device that converts from octal to binary number is called

    (a) Decoder   (b) Multiplexer   (c) Encoder   (d) De-multiplexer

4. A comparator is a special combinational circuit designed primarily to compare the relative magnitude of _____ numbers .

    (a) two decimal   (b) three decimal   (c) two binary   (d) three binary

5. ------------------ is used for the purpose of detecting errors during transmission of binary information

    (a) Message bit   (b) Carry bit   (c) Parity bit   (d) Selection bit

6. D flip-flop during the occurrence of clock pulse if ____, the output ____ and if ____, the output is reset.

    (a) D = 0, Q = 0 , D is set   (b) D = 1, Q = 1 , D = 0

    (c) D = 1, Q is set , D = 0   (d) None of these

7. State assignments are used to avoid _____

    (a) Static – 0 hazard   (b) Races

    (c) Static – 1 hazard   (d) Dynamic hazards

8. _____consists of a set of fixed AND gates connected to a decoder and a programmable OR array.

    (a) EPROM   (b) EEPROM   (c) PROM   (d) EAPROM

9. Flash memories are similar to

    (a) ROM   (b) PROM   (c) RAM   (d) EEPROM

10. _____ is the minimum time required to maintain a constant voltage levels at the excitation inputs of the flip-flop device.

    (a) Rise time   (b) Fall time

    (c) Setup time   (d) None of these

PART - B (5 x 2 = 10 Marks)

11. Obtain the canonical SOP form of the function Y=AB+ACD.

12. Define Multiplexer and draw its block diagram.

13. List out the applications of Flip Flops.

14. Define Glitch.

15. What is meant by PLA?

PART - C (5 x 16 = 80 Marks)

16. (a) Use Quine McClusky method to obtain the minimal sum for the following function. $F (X_1 X_2 X_3 X_4) = \sum (0, 1, 3, 6, 7, 14, 15)$.   (16)

Or

(b) (i) Give a brief note on Weighted codes.   (8)

    (ii) If $\bar{A}B + C\bar{D} = 0$ then. Prove that $AB + \bar{C}(\bar{A} + \bar{D}) = AB + BD + \bar{B}\bar{D} + \bar{A}\bar{C}D$.   (8)

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17. (a) (i) Compare the characteristics of different Logic families. (8)

(ii) Design a 4-bit Parallel Adder/Subtractor using logic gates. (8)

Or

(b) (i) Discuss the 4-bit Magnitude comparator with its logic diagram. (8)

(ii) Write the truth table of a three - to - eight lines decoder and construct the circuit for 3 - to - 8 lines decoder. (8)

18. (a) Explain the operation universal shift register with logic diagram. (16)

Or

(b) Define Counter. Design a Synchronous decade counter using JK flip flop. (16)

19. (a) What do meant by hazards? Describe hazards in combinational and sequential circuits with suitable examples. (16)

Or

(b) Write short notes on: (i) Races (ii) Hazards. (16)

20. (a) What is RAM. Explain in detail about the types of RAM with necessary logic diagrams. (16)

Or

(b) (i) With a neat sketch, explain the block diagram of PLA. (8)

(ii) Draw the logic diagram of a 4×4 RAM. (8)

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