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**Question Paper Code: 31536**

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2016

Third Semester

Electronics and Instrumentation Engineering

01UEI306 – DIGITAL ELECTRONICS

(Regulation 2013)

Duration: Three hours

Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. What is 8421 code?
2. Show that an Ex-NOR circuit produces POS form.
3. Construct a 4x1 multiplexer using 2x1 multiplexers.
4. Distinguish combinational circuits with sequential circuits.
5. Compute the excitation table of T flip flop.
6. Compare the characteristics of latches with flip flops.
7. Define static and dynamic hazards.
8. What is race conditions?
9. List any four application of PLA.
10. Compare EPROM with EEPROM.

PART - B (5 x 16 = 80 Marks)

11. (a) Compute the minimized Boolean expression using K-map

$$F = A'BC'D' + A'BC'D + ABC'D' + AB'C'D + A'B'CD'$$

(16)

Or

- (b) Compute the minimized Boolean expression using tabulation method  
 $F = \Sigma(1, 4, 6, 7, 8, 9, 10, 11, 15)$  (16)

12. (a) Design a combinational logic using a suitable multiplexer to realize the Boolean expression:  $F = AD' + B'C + BC'D$ . (16)

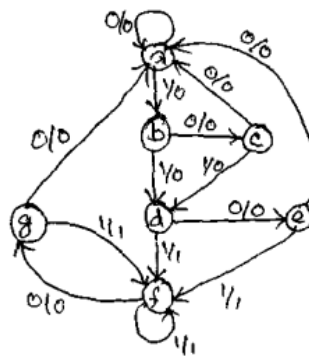
Or

- (b) Design a BCD to Excess-3 converter using truth table and k-map simplification. (16)

13. (a) Design a mod-7 synchronous binary counter using JK flip-flops. (16)

Or

- (b) Reduce the given state diagram and justify that both the diagrams are equal. (16)



14. (a) Design a asynchronous sequential circuit specified by the following flow table. (16)

	00	01	10	10
A	A,0	A,0	A,0	B,0
B	A,0	A,0	B,1	B,1

Or

- (b) Illustrate the concept of race free state assignment with suitable examples. (16)

15. (a) (i) Construct a PAL logic circuit for the following functions,  
 $X = A'B'C + AB'C' + B'C$   $Y = A'B'C + AB'C'$ . (8)

- (ii) Construct a logic circuit with a PLA having 3 inputs and 3 product terms and two outputs.

$$F1 = \Sigma(1, 3, 5)$$

$$F2 = \Sigma(5, 6, 7)$$
 (8)

Or

- (b) Discuss about static and dynamic RAM cell. (16)