Reg. No. : | | | | | | | | | | |

Question Paper Code: 31754

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2016

Seventh Semester

Electronics and Instrumentation Engineering

01UEI704 - VLSI SYSTEM DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. Compare enhancement and depletion mode devices.
2. What is body effect?
3. What is lambda design rule?
4. Define short channel devices.
5. Draw the CMOS implementation of 4-to-1 MUX using transmission gates.
6. What are the advantages of AOI implementation of two level logic functions?
7. What is meant by routing? What are its different phases?
8. What are the advantages of PLA?
9. What are the different design units in VHDL?
10. What is the use of block statements in VHDL?

PART - B (5 x 16 = 80 Marks)

11. (a) Derive the expression for current equation for NMOS transistor. (16)

Or

(b) Illustrate the steps involved in the fabrication of twin tub C-MOS process. (16)

12. (a) Draw the CMOS inverter transfer characteristics and explain its operation, clearly indicating the various regions. (16)

Or

(b) Derive the expression for 4:1 and 8:1 pull up and pull down ratios of nMOS inverter. (16)

13. (a) Explain with neat diagrams the design of 4:1 multiplexer using dynamic CMOS and Domino logic. (16)

Or

(b) Explain the design and working of carry look ahead adder. (16)

14. (a) Explain the general architecture of FPGA and bring about different programmable blocks used. (16)

Or

(b) Explain in detail about planning placement and routing techniques of FPGA. (16)

15. (a) Write a VHDL code to realize the behavioral model and data flow model of a full adder. (16)

Or

(b) Write a VHDL code to realize the 4-bit synchronous counter using structural modeling. (16)