Reg. No. : | | | | | | | | | | |

Question Paper Code: 51233

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2016

Third Semester

Computer Science and Engineering

15UCS303 - COMPUTER ORGANIZATION AND ARCHITECTURE

(Common to Information Technology)

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. The control unit controls other units by generating _____ .

   (a) Control signals (b) Timing signals
   (c) Transfer signals (d) Command signals

2. The addressing mode, where you directly specify the operand value is _____.

   (a) Immediate (b) Direct (c) Definite (d) Relative

3. A floating point number that has a O in the MSB of mantissa is said to have _____

   (a) Overflow (b) Underflow
   (c) Important number (d) Undefined

4. The periods of time when the unit is idle is called as _____.

   (a) Stalls (b) Bubbles (c) Hazards (d) Both (a) and (b)

5. Cache memory works on the principle of _____.

   (a) Locality of data (b) Locality of memory
   (c) Locality of reference (d) Locality of reference and memory

PART - B (5 x 2 = 10 Marks)

6. State the different types of instrucion formats. Give example.

7. What are the various types of operations required for instructions?

8. List out the advantages of using Booth algorithm.

9. What are the classifications of data hazards? Define it.

10. Distinguish between asynchronous DRAM and synchronous RAM.

PART - C (5 x 16 = 80 Marks)

11. (a) (i) Describe the typical special registers available in processor. (8)

(ii) Describe the functional units of computer. (8)

Or

(b) Illustrate different types of addressing modes with suitable example. (16)

12. (a) (i) Multiply +13 and -6 using Booth's multiplication algorithm. (8)

(ii) Divide 1000 by 11 using restoring division algorithm. (8)

Or

(b) Explain addition and subtraction operations of signed numbers in detail. (16)

13. (a) What is data hazard? Explain the methods for dealing with the data hazards. (16)

Or

(b) Summarize the concept of superscalar processor operations in detail. (16)

14. (a) Explain various memory technologies with a suitable example. (16)

Or

(b) Describe the different types of mapping schemes of cache memory. (16)

15. (a) Explain the virtual memory address translation and TLB with necessary diagram. (16)

Or

(b) Discuss direct memory access in detail. (16)