Reg. No. : | | | | | | | | | | |

Question Paper Code: 52332

M.E. DEGREE EXAMINATION, NOV 2016

Third Semester

Computer Science and Engineering

15PCS301 - MULTI CORE ARCHITECTURE

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (5 x 1 = 5 Marks)

1. The time taken between memory access and sharing resources is called as

   (a) Access time (b) Cycle time
   (c) Memory bandwidth (d) Clock cycles

2. Multiple processors concurrently operate on a model called

   (a) Latency model (b) Shared memory model
   (c) Single Model (d) Resource Model

3. GPU Architecture stands for

   (a) Graphics Processing Unit (b) Geo Processing Unit
   (c) General Preparation Unit (d) Graphics Preparing Unit

4. Cache memory placed between

   (a) RAM & CPU (b) ROM & CPU
   (c) CPU & hard disk (d) CPU & pen drive

5. Open mp programs that applied for looping statements that contains

   (a) Private class (b) Public class
   (c) Static class (d) Independent class

PART - B (5 x 3 = 15 Marks)

6. Differentiate the SMT and CMP Architecture.

7. What is meant by Multi stage Interconnection networks?

8. Differentiate the Intel and IBM cell Architecture.

9. Recall and write the different technologies.

10. Develop a simple open mp program.

PART - C (5 x 16 = 80 Marks)

11. (a) Organize the ideas of ILP and explain its types , limitations with necessary diagrams. (16)

Or

(b) Discuss about the limitations of single core architecture. (16)

12. (a) Classify the types of memory consistency models and explain in detail. (16)

Or

(b) Write the limitations in Symmetric shared memory multiprocessor and snooping protocols. (16)

13. (a) Organize the ideas of homogenous and heterogeneous architecture with neat diagrams. (16)

Or

(b) Design the Graphical user device using GPU. (16)

14. (a) Use the optimization techniques in memory hierarchy develop the primary memory architecture. (16)

Or

(b) Explain in detail the schemes available for enforcing coherence. Discuss its implementation techniques with suitable state diagrams. (16)

15. (a) Organize the different programming models in multicore programming. (16)

Or

(b) Develop a MP program for parallel programming models. (16)