Reg. No. : | | | | | | | | | | |

Question Paper Code: 51228

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2016

Second Semester

Computer science and Engineering

15UCS208 - DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. How many bits are required to represent the decimal numbers in the range 0 to 999 using straight binary code

   (a) 8 (b) 10 (c) 12 (d) 16

2. What is the algebraic function of Exclusive-OR gate

   (a) F=xy1 + x1y (b) F=xy +x1y1 (c) F=x1y1 + x1y (d) F=x1y 1+x1y1

3. How many binary outputs would a 3 digit BCD-to-Binary converter have

   (a) 12 Outputs (b) 24 Outputs (c) 3 Outputs (d) 9 Outputs

4. Which one is not the basic type of programmable logic devices?

   (a) Read only memory (b) Programmable logic Array
   (c) Programmable Array Logic (d) Read memory

5. In PAL , how 10L8 is represented

   (a) 10-I/P L-Active Low Output 8 Outputs
   (b) 10-I/P L-Active Low Input 8 Outputs
   (c) 10-I/P L-Active Low Input Output 8 Outputs
   (d) none of these

6. Convert $(4021.2)_5$ to its equivalent decimal

(a) $(112.4)_{10}$ (b) $(512.4)_{10}$ (c) $(521.4)_{10}$ (d) $(511.4)_{10}$

7. What is a latch?

(a) Memory device with clock signal
(b) Memory device without clock signal
(c) Memory device without Input signal
(d) Memory device with clock signal

8. A counter has 14 stable states 0000 through 1101. If the input frequency is 50KHz what will be its output frequency?

(a) 4.57 KHz (b) 2.57 KHz (c) 6.54 KHz (d) 3.57 KHz

9. This is the equation of Q(t+1)=S+R'Q

(a) D Flip-flop (b) JK Flip - Flop
(c) SR Flip-Flop (d) T Flip - Flop

10. In which hazard, the output may momentarily go to 0 when it should remain1.

(a) Static1-hazard (b) Static11-hazard
(c) Static 0-hazard (d) Static 00-hazard

PART - B (5 x 2 = 10 Marks)

11. State and prove the consensus theorem.

12. Implement half adder using NAND Gates.

13. Draw the logic diagram of a one to four line de-multiplexer.

14. Give the truth table of T-flip flop.

15. What is the difference between synchronous and asynchronous sequential circuits?

PART - C (5 x 16 = 80 Marks)

16. (a) Define K-Map. Plot the expression on K-map:
$F(w, x, y)=\sum m(0, 1, 3, 5, 6) + d(2, 4)$ (16)

Or

(b) Reduce the following:

(i) A (A + B) (4)

(ii) A'B'C' + A'BC' + A'BC (6)

(iii) AB + (AC)' + AB'C (AB + C) (6)

17. (a) Write HDL behavioural description of 4bit comparator with 6bit output y[5:0]. Bit 5 of y-> equal, bit 4-> unequal, bit 3->>, bit 2-><, bit 1->>=, bit0-><=. (16)

Or

(b) (i) Write down the steps in implementing a boolean function with levels of NAND gates. (8)

(ii) Draw the truth table and circuit diagram of 4 to 2 encoder. (8)

18. (a) Write a behavioral model for 1:4 DeMux using Verilog HDL. (16)

Or

(b) How does an encoder differ from a decoder?. (16)

19. (a) Describe D-Flipflop with an example. (16)

Or

(b) Define shift register. Mention the types of shift register with examples. (16)

20. (a) What are two techniques are available in critical race free state assignment? (16)

Or

(b) Design an asynchronous sequential circuit with inputs xl and x2 and one output z. Initially and at any time if both the inputs are 0, output is equal to 0. When xl or x2 becomes 1, z becomes 1. When second input also becomes 1, z = 0; The output stays at 0 until circuit goes back to initial state. (16)

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