**Reg. No. :** | | | | | | | | | | |

# Question Paper Code: 41227

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2016

Second Semester

Computer Science and Engineering

14UCS207 – DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 1 = 10 Marks)

1. Convert $10101_2$ to decimal

   (a) 16 (b) 21 (c) 19 (d) 20

2. $AB+AB'=$

   (a) $A$ (b) $B$ (c) 0 (d) 1

3. Parallel adder is

   (a) Sequential circuits
   (b) Combinational circuits
   (c) Either sequential or Combinational circuits
   (d) Neither sequential nor Combinational circuits

4. Which gate is best used as a basic comparator?

   (a) AND (b) OR (c) XOR (d) XNOR

5. A demultiplexer is used to ----------

   (a) perform arithmetic division
   (b) select data from several inputs and route it to a single output
   (c) steer the data from a single input to one of the many outputs
   (d) perform parity checking

6. HDL stands for

(a) Hardware Description Language (b) Hardware Design Language
(c) High Design Language (d)High Description Language

7. The basic shift register operations are
(a) serial in serial out (b) serial in parallel out
(c) parallel in serial out (d) all the above

8. Flip flop is to

(a)Store octal value (b) Store hexadecimal value
(c) Binary value (d) ACCII value

9. ---------- exist when two or more binary state variables changes value in reponse to change in an input variable.
(a) Race (b) Hazards
(c) Cycles (d) None of these

10. _____unwanted switching transients that may appear at the output of a circuit is known as

(a) Hazards (b) Cycles (c) Races (d) Critical Race

PART - B (5 x 2 = 10 Marks)

11. Show that the dual of the exclusive-OR is equal to its complement.

12. Draw a half subtractor and write the corresponding truth table.

13. Implement the following function using 4 X 1 MUX.

$F(a, b, c) = \Sigma(1,3,5,7)$.

14. List the important of features of HDL language.

15. List the need for state reduction in sequential logic design.

PART - C (5 x 16 = 80 Marks)

16. (a) Reduce the following expression to the SOP and POS form

$$Y(W, X, Y, Z) = \sum m(1, 2, 3, 5, 9, 12, 14, 15) + \sum d(4, 8, 11).$$ (16)

Or

(b) (i) Simplify the following Boolean expression to a minimum number of literals
X' Y + XY + XZ' + XY'Z'. (8)

(ii) The state of a 12 cell register is 010110010111. What is its content if it represents.
(1) Three decimal digit in BCD
(2) Three decimal digit in excess 3 code
(3) Three decimal digit in 2521 code
(4) Three decimal digit in 84 – 2 – 1 code. (8)

17. (a) (i) Design a combinational circuit with three inputs and one output. The output is 1 when the binary value of the inputs is less than or equal to 3. The output is 0 otherwise. (10)

(ii) Design a four bit parallel adder circuit. (6)

Or

(b) (i) Design a 4-bit magnitude comparator with neat diagram. (12)

(ii) List the features of HDL language. (4)

18. (a) (i) Implement the following Boolean function with a 4:1 multiplexer and external gates.
$F(A, B, C, D)=\sum(1, 3, 4, 11, 12, 13, 14, 15)$. (8)

(ii) Using a decoder and external gates, design the combinational circuits defined by the following three Boolean functions:
$F1=x'y'z' +xz +yz$
$F2=xy'z' + x'y$
$F3=x'y'z + xy$ (16)

Or

(b) Design a BCD to Excess 3 code converter using PROM. (16)

19. (a) A sequential circuit has two flip flops (A and B), two inputs (x and y) and an output (Z). The flip flop input functions and the circuit output function are as follows.
JA = XB + y'B KA = xy'B'
JB = xA' KB = xy' + A
Z = xyA + x'y'B
Obtain the logic diagram; sate table, state diagram and state equations. (16)

Or

(b) (i) With neat diagram, explain the operation of 4-bit Universal Shift Register. (12)

(ii) Write HDL code for T Flip-flop. (4)

20. (a) Design an asynchronous sequential circuit with two inputs *X* and *Y* and with one output *Z*. Whenever *Y* is 1, input *X* is transferred to *Z*. When *Y* is 0, the output does not change for any change in *X*. Use D- Flip flop for implementation of the circuit. (16)

Or

(b) Write short notes with an example for

(1) Shared row state assignment

(2) One hot state assignment (16)