Reg. No. : | | | | | | | | | | |

Question Paper Code: 31227

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2016

Second Semester

Computer Science and Engineering

01UCS207- DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Which gates are called as the universal gates? What are their advantages?
2. Subtract $(1010)_2$ from $(1000)_2$ using 2's complement method.
3. What is binary adder? Draw its logical diagram?
4. Write a gate level HDL description for the full adder circuit.
5. Differentiate between multiplexer and demultiplexer.
6. Determine the number of address lines required for accessing 2MB and a 64KB memory.
7. Give the classification of PLDs.
8. State the differences between combinational logic and sequential logic.
9. What is the operation of T flip-flop? Illustrate using truth table.
10. List the assumptions that must be made for a fundamental mode circuit.

PART - B (5 x 16 = 80 Marks)

11. (a) Reduce the following function using K-map technique and implement the reduced Boolean expression with basic gates

$f(A, B, C, D) = \pi M (0, 3, 4, 7, 8, 10, 12, 14) + d (2, 6)$. (16)

Or

(b) Find the minimal sum of products for the Boolean expression, $F(w, x, y, z) = \sum m (1, 3, 4, 5, 9, 10, 11) + \sum d (6, 8)$ using Quine–Mc Cluskey tabulation method. (16)

12. (a) Design a combinational circuit that convert a 4-bit BCD number into 4-bit Excess-3 number. (16)

Or

(b) (i) Explain in detail the various carry propagation adder with suitable diagram. (10)

(ii) Write down the HDL code for data flow description of 4-bit adder. (6)

13. (a) (i) Implement the function, $F(A, B, C, D) = \sum m (0, 1, 2, 5, 6, 9, 12, 14)$ using two 4x1 multiplexers. (8)

(ii) Write a structural Verilog description for a 2x4 decoder with a neat sketch. (8)

Or

(b) A combinational logic circuit is defined by the following functions:

$F_1 (x, y, z) = \sum m (1, 2, 4, 6)$

$F_2 (x, y, z) = \sum m (0, 1, 6, 7)$

$F_3 (x, y, z) = \sum m (2, 6)$

$F_4 (x, y, z) = \sum m (1, 2, 3, 5, 7)$

Implement the circuit using a PLA with 3 inputs, 7 product terms and 4 outputs. (16)

14. (a) (i) Write the procedure for analyzing a clocked sequential circuit with JK flip flop. (8)

(ii) Design a sequential mod-7 counter. (8)

Or

(b) (i) Explain in detail about parallel in serial out shift register, with neat sketches. (10)

(ii) Write the HDL for full adder circuits. (6)

15. (a) (i) Describe the design procedure for asynchronous sequential circuits. (10)

(ii) Write short notes on ASM chart. (6)

Or

(b) (i) Briefly describe about race free assignment in asynchronous sequential circuits. (8)

(ii) Write short notes on hazards in combinational and sequential circuits. (8)