Reg. No. : | | | | | | | | | | |

Question Paper Code: 43062

B.E. / B.Tech. DEGREE EXAMINATION, DEC 2020

Third Semester

Instrumentation and Control Engineering

14UIC302 – DIGITAL LOGIC CIRCUITS AND DESIGN

(Regulation 2014)

Duration: One hour Maximum: 30 Marks

PART A - (6 x 1 = 6 Marks)

(Answer any six of the following questions)

1. What is A.1

   (a) 1 (b) A’ (c) 0 (d) A+A

2. The Hexadecimal equivalent of a decimal number 48 is

   (a) 2B (b) 2E (c) 2F (d) F2

3. Write the Boolean equation for the SUM output of a full adder.

   (a) $A \oplus B \oplus C$ (b) A + B + C (c) $\overline{A} \oplus \overline{B} \oplus \overline{C}$ (d) $\overline{A} + \overline{B} + \overline{C}$

4. In PROM, we can

   (a) Store the data once and read multiple times
   (b) Store and erase data once
   (c) Store and erase data multiple times
   (d) Store once and read once

5. How many flipflops are required to build a binary counter that counts from 0 to 1023?

(a) 12 (b) 20 (c) 50 (d) 10

6. Which type of gate can be used to add two bits?

(a) Ex-OR (b) Ex-NOR (c) Ex-NAND (d) NOR

7. In ASM, the decision box is represented by

(a) circle (b) oval (c) diamond (d) rectangle

8. Which element is used to avoid static hazard?

(a) SR Latch (b) MUX (c) Decoder (d) none of the above

9. The VHDL is based on the _____ library

(a) IEE (b) WORK (c) IEEE (d) Standard

10. I^2L operation is similar to

(a) TTL (b) RTL (c) ECL (d) CMOS

PART – B (3 x 8= 24 Marks)

(Answer any three of the following questions)

11. Estimate the prime implicants for the following expression $F = \Sigma$ (1, 4, 6, 7, 8, 9, 10, 11, 15). Use tabulation method. (8)

12. Construct and explain an expression tree with an example. (8)

13. Construct a decade ripple counter using flip flops and explain. (8)

14. Explain with neat diagram the different hazards and the way to eliminate them. (8)

15. What is VHDL? Design a full adder circuit using VHDL code. (8)