Reg. No.:					

Question Paper Code: 31362

B.E. / B.Tech. DEGREE EXAMINATION, DEC 2020

Third Semester

Instrumentation and Control Engineering

	01U	JIC302 – DIGITAL LO	OGIC CIRCUITS	S AND DI	ESIGN			
		(Regu	ulation 2013)					
Г	Ouration: One hour	r		Ma	aximum: 30 Marks			
		PART A -	$(6 \times 1 = 6 \text{ Marks})$	s)				
		(Answer any six o	f the following o	questions))			
1.	The Hexadecimal equivalent of a decimal number 48 is							
	(a) 2B	(b) 2E	(c) 2F		(d) F2			
2. How many outputs are on a BCD decoder?								
	(a) 4	(b) 16	(c) 8		(d) 10			
3.	What is ROM?							
(a) repeat on memory			(b) read on memory					
	(c) read only	memory	(d) repeat only memory					
4.	In PROM, we ca	n						
(a) store the data once and read multiple(c) store and erase data multiple times			•	` '	tore and erase data once tore once and read once			
5.	Which type of ga	ate can be used to add t	wo bits?					
	(a) Ex-OR	(b) Ex-NOR	(c) Ex-NA	ND	(d) NOR			
6.	How many flipfle	ops are required to buil	d a binary count	er that cou	ants from 0 to 1023	?		
	(a) 12	(b) 20	(c) 50		(d) 10			

7.	The next state variables in asynchronous sequential circuits are called							
	(a) secondary v(c) primary var		` ´	(b) excitation variables(d) short term memory				
8.	In ASM, the decision	on box is represented	by					
	(a) circle	(b) oval	(c) diamond	(d) rectan	gle			
9.	Which of the follow	wing logic family has	the shortest propagatio	n delay?				
	(a) CMOS	(b) NMOS	(c) ECL	(d) 74Sxx				
10.	The VHDL is base	d on thelib	rary					
	(a) IEE	(b) WORK	(c) IEEE	(d) Standa	ard			
		PART - B (2)	3 x 8= 24 Marks)					
		(Answer any three o	f the following question	ons)				
11.		0 0	ion method and reali , 12, 10, 8, 6, 4, 3, 2	•	l function (8)			
12.	Design full ad function using		ubtractor circuit using	logic gates and	explain it			
13.	With a neat dia	gram explain the wor	king of a master–slave	JK flip flop.	(8)			
14.	List and explai	n the steps used for ar	nalyzing an asynchrono	ous sequential circ	cuit. (8)			
15.	Explain with th	ne aid of a circuit diag	ram, the operation of a	TTL 3-input NA	MD gate. (8)			