Reg. No. : | | | | | | | | | | |

Question Paper Code: 43306

B.E. / B.Tech. DEGREE EXAMINATION, DEC 2020

Third Semester

Electrical and Electronics Engineering

14UEE306 – DIGITAL LOGIC CIRCUITS

(Regulation 2014)

Duration: 1.15 hrs Maximum: 30 Marks

PART A - (6 x 1 = 6 Marks)

(Answer any six of the following questions)

1. Convert $(10111.10)_2$ to decimal equivalent

   (a) $(23.5)_{10}$ (b) $(46.5)_{10}$ (c) $(23.2)_{10}$ (d) $(46.2)_{10}$

2. How many binary numbers are created with 8 bits?

   (a) 128 (b) 256 (c) 64 (d) 32

3. How many select lines are contained in multiplexer with 1024 inputs and one output

   (a) 20 (b) 10 (c) 15 (d) 28

4. AND-OR realization is equivalent to

   (a) SOP (b) POS (c) K-map (d) None of these

5. Race around condition occurs in JK flip-flop if

   (a) J=1,K=1 (b) J=0,K=0 (c) J=0,K=1 (d) J=1,K=0

6. In the toggle mode a JK flip-flop has

   (a) J = 0, K = 0 (b) J = 1, K = 1 (c) J = 0, K = 1 (d) J = 1, K = 0

7. Which of the following is a type of shift register counter?

(a) Decade (b) Binary (c) Ring (d) BCD

8. Which of the statement is true about static-1 hazard?

(a) output goes momentarily goes to 0 when it should remain at 1
(b) output goes momentarily goes to 1 when it should remain at 0
(c) output changes 3 or more times
(d) none of these

9. The example of sequential circuit is

(a) Counter (b) 7-segment display
(c) Combinational logic circuit (d) Shift register

10. Main component of a VHDL description are

(a) Entry and Package (b) Entry and Architecture
(c) Package and Architecture (d) Package and Configuration

PART – B (3 x 8= 24 Marks)

(Answer any three of the following questions)

11. Explain Gray code and Binary code. (8)

12. Design a full adder using two half-adders and an OR gate. (8)

13. Design a synchronous counter to count the sequence 0 - 1 - 2 - 4 5 - 6 - 0 using JK flip flop. (8)

14. Explain the various types of hazards in sequential circuit design and methods to eliminate them. Give suitable examples. (8)

15. Explain the structural VHDL description for a 2 to 4 decoder in details. (8)