Reg. No. : | | | | | | | | | | |

Question Paper Code: 43402

B.E. / B.Tech. DEGREE EXAMINATION, DEC 2020

Third Semester

Electronics and Communication Engineering

14UEC302 – DIGITAL ELECTRONICS AND DESIGN

(Regulation 2014)

Duration: 1.15 hrs Maximum: 30 Marks

PART A - (6 x 1 = 6 Marks)

(Answer any six of the following questions)

1. The binary equivalent of decimal 41 is

   (a) 101001 (b) 101010 (c) 010111 (d) 101101

2. The simplified logic of the Boolean function $x'y'z + x'yz + xy'$ is

   (a) $x'yz+xyz$ (b) $x'z + xy'$ (c) $x'z'+ x'y'$ (d) $xz+xy$

3. The difference output of half-subtractor is

   (a) $x'y'+ xy$ (b) $xy+xy'$ (c) $xy+xy'$ (d) $x'y+xy'$

4. The circuit that generates the parity bit in the transmitter is

   (a) Parity checker (b) Parity generator

   (c) Both (a) and (b) (d) None of these

5. Which latch is called a transparent latch

   (a) SR latch (b) JK latch (c) D latch (d) T latch

6. How many flip-flops are needed for a 4-bit counter?

   (a) 2 (b) 3 (c) 4 (d) 6

7. The voltage needed for a TTL IC power supply is

(a) 5V dc (b) 10 V dc (c) 2 V dc (d) 20 V dc

8. Which of the following memories in non-volatile memory?

(a) ROM (b) PROM
(c) Ferrite core memory (d) None of these

9. A circuit which do not operate in synchronous with clock signal is

(a) Synchronous sequential circuits (b) Asynchronous sequential circuits
(c) FPGA (d) combinational circuits

10. In this mode the inputs and outputs are represented by levels

(a) Fundamental mode (b) Pulse mode
(c) Both (a) and (b) (d) None of these

PART – B (3 x 8= 24 Marks)

(Answer any three of the following questions)

11. Realize the following function as Multilevel NAND –NAND gate and Multilevel NOR –NOR gate

$F = \bar{A}\,B + B\,(C + D) + E\bar{F}\,(\bar{B} + \bar{D})$ (8)

12. With logic diagram Truth table and explain about 3-to-8 decoder. (8)

13. With neat diagram explain in detail about how the race around condition is avoided in master-slave JK flip-flop. (8)

14. With block diagram explain about PLA and realize the following functions in PLA:

$F1 = \bar{A}\ B\ \bar{C} + A\ \bar{B}\ C + \bar{A}\ B\ C$

$F2 = A\ B + AC + \bar{A}BC$ (8)

15. Develop VHDL code for 3 to 8 decoder. (8)