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Question Paper Code: 33402

B.E. / B.Tech. DEGREE EXAMINATION, DEC 2020

Third Semester

Electronics and Communication Engineering

01UEC302 - DIGITAL ELECTRONICS AND DESIGN

(Regulation 2013)

Duration: One hour

Maximum: 30 Marks

PART A - $(6 \times 1 = 6 \text{ Marks})$

(Answer any six of the following questions)

1.	The binary equivalent of decimal 41 is				
	(a) 101001	(b) 101010	(c) 010111	(d) 101101	
2.	The simplified logic o	The simplified logic of the Boolean function $x'y'z + x'yz + xy'$ is			
	(a) <i>x'yz+xyz</i>	(b) $x'z + xy'$	(c) $x'z' + x'y'$	(d) $xz+xy$	
3.	The difference output of half-subtractor is				
	(a) $x'y' + xy$	(b) $xy+xy'$	(c) $xy+xy'$	(d) $x'y+xy'$	
4.	The circuit that generates the parity bit in the transmitter is				
	(a) Parity checker	(b) Parity get	nerator		
	(c) Both (a) and (b	b) (d) None of t	these		
5.	Which latch is called a transparent latch				
	(a) SR latch	(b) JK latch	(c) D latch	(d) T latch	
6.	How many flip-flops are needed for a 4-bit counter?				
	(a) 2	(b) 3	(c) 4	(d) 6	

7. The voltage needed for a TTL IC power supply is

(a) 5V dc (b) 10 V dc (c) 2 V dc (d) 20 V dc

8. Which of the following memories in non-volatile memory?

(a) ROM	(b) PROM
(c) Ferrite core memory	(d) None of these

9. A circuit which do not operate in synchronous with clock signal is

(a) Synchronous sequential circuits	(b) Asynchronous sequential circuits
(c) FPGA	(d) combinational circuits

- 10. In this mode the inputs and outputs are represented by levels
 - (a) Fundamental mode (b) Pulse mode
 - (c) Both (a) and (b) (d) None of these

PART - B (3 x 8= 24 Marks)

(Answer any three of the following questions)

- 11. Simplify the following expression $F(w, x, y, z) = \sum_{m} (1, 3, 4, 5, 9, 10, 11) + \sum_{d} (6, 8)$ using Quine – McCluskey method. (8)
- 12. Implement the full subtractor using a 1: 8 demultiplexer. (8)
- 13. Discuss in detail about JK flip flop with its truth table, state diagram and characteristics equation. (8)
 14. Implement the following two Boolean functions
- F1(A,B,C) = $\sum(0,1,2,4)$ F2(A,B,C) = $\sum(0,5,6,7)$ using i) PLA ii) PAL iii) ROM (8)
- 15. Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 1, input X is transferred to Z. When Y is 0, the output does not change for any change in X. Use SR latch for implementation of the circuit.

(8)