Reg. No. :

Question Paper Code: 56403

B.E. / B.Tech. DEGREE EXAMINATION, DEC 2020

Sixth Semester

Electronics and Communication Engineering

15UEC603- VLSI DESIGN

(Regulation 2015)

Duration: 1.15 hrs   Maximum: 30 Marks

PART A - (6 x 1 = 6 Marks)

(Answer any six of the following questions)

1. In continuous assignment left hand side must be   CO1-R

    (a) Net   (b) Reg   (c) Scalar or vector net   (d) Scalar or vector reg

2. The primary mechanisms for modeling the behavior of a Verilog   CO1- R
    design needs

    (a) Initial statement   (b) Always statement   (c) Both (a) and (b)   (d) Only (a)

3. CMOS technology is used in developing   CO2-U

    (a) Microprocessors   (b) Microcontrollers

    (c) Digital logic circuits   (d) all of the mentioned

4. In CMOS fabrication, the photoresist layer is exposed to   CO2- R

    (a) visible light   (b) infra red light   (c) ultraviolet light   (d) fluorescent

5. In CMOS circuits, which type of power dissipation occurs due to   CO3-U
    switching of transient current and charging & discharging of load
    capacitance?

    (a) Static dissipation   (b)Dynamic dissipation

    (c) Both a and b   (d) None of the above

6. The number of pass transistors connected in series can be increased if   CO3- R

    (a) Compressor is connected   (b) Ground is connected

    (c) Voltage regulator is connected   (d) Buffer is connected

7. Charge leakage and noise margin problems can be addressed by adding _____ CO4-U

   (a) Keeper circuit   (b) domino gate   (c) pass transistor   (d) transmission gate

8. In CMOS NAND gate, p transistors are connected in   CO4- R

   (a) Series   (b) Parallel   (c) Cascade   (d) Random

9. The number of test vectors for exhaustive testing is calculated by   CO5-A

   (a) $2^{(m+n)}$ (b) $2^{((m+n)/2)}$ (c) $2^{(m-n)}$ (d) $2^{2(m+n)}$

10. The process of removing equivalent faults is called as   CO5- R

    (a) Equivalent removing   (b) Fault collapsing

    (c) Fault reduction   (d) Bulk damaging

PART – B (3 x 8= 24 Marks)

(Answer any three of the following questions)

11. Write a Verilog program for 2 to 4 decoder in dataflow modeling and behavioral modeling.   CO1-U   (8)

12. Explain in detail DC transfer characteristic of CMOS inverter   CO2-U   (8)

13. Analyze the static and dynamic power dissipation in CMOS circuits with necessary diagrams and expressions.   CO3-Ana   (8)

14. Discuss the comparison of circuit families   CO4 -U   (8)

15. Describe the scan based approaches and built in self-test to design for testability in detail.   CO5- U   (8)

56403