Reg. No. : | | | | | | | | | | |

Question Paper Code: 46404

B.E. / B.Tech. DEGREE EXAMINATION, DEC 2020

Sixth Semester

Electronics and Communication Engineering

14UEC604-VLSI DESIGN

(Regulation 2014)

Duration: 1.15 hrs Maximum: 30 Marks

PART A - (6 x 1 = 6 Marks)

(Answer any six of the following questions)

1. VLSI technology uses _____to form integrated circuit.

   (a) Transistors (b) Switches (c) Diodes (d) Buffers

2. The difficulty in achieving high doping concentration leads to

   (a) Error in concentration (b) Error in variation
   (c) Error in doping (d) Distribution

3. In accordance to the scaling technology , the total delay of the logic circuit depends on
   (a) The capacitor to be charged
   (b) The voltage through which capacitance must be charged
   (c) Available current
   (d) All of the above

4. In CMOS circuits, which type of power dissipation occurs due to switching of transient current & discharging of load capacitance?

   (a) Static dissipation (b) Dynamic dissipation
   (c) Both a and b (d) None of the above

5. The output of latches will remain in set/reset until
   (a) The trigger pulse is given to change the state
   (b) Any pulse given to go into previous state
   (c) They don't get any pulse more
   (d) None of the Mentioned

6. The sequential circuit is also called

   (a) Flip-flop (b) Latch (c) Strobe (d) None of the Mentioned

7. Boundary scan test is used to test

   (a) Pins (b) Multipliers (c) Boards (d) wires

8. CMOS domino logic occupies

   (a) Smaller area (b) Larger area

   (c) Both of the mentioned (d) None of the mentioned

9. Test Benches procedure is _____

   (a) Smaller design (b) Larger design

   (c) Complicated (d) None of the mentioned

10. Blocking & Non blocking assignment is

   (a) =statement & ≤ statement (b) ≤ statement
   (c) Statement (d) ≥ statement & =statement

PART – B (3 x 8= 24 Marks)

(Answer any three of the following questions)

11. Explain layout design rules in detail. (8)

12. Explain in detail about delay estimation, logical effort and transistor sizing with example. (8)

13. Explain in detail: (i) Conventional CMOS Latch (ii) Conventional CMOS Flip flop. (8)

14. What are the various testing methods to be considered while designing a VLSI circuit? (8)

15. Explain the concept involved in structural gate level modeling and also give the description for Decoder and parity encoder. (8)