Reg. No.:					

Question Paper Code: 37404

B.E. / B.Tech. DEGREE EXAMINATION, DEC 2020

Seventh Semester

Electronics and Communication Engineering

01UEC704 - EMBEDDED AND REAL TIME SYSTEMS

		(Reg	gulation 2013)				
Duration: One hour			Maximum: 30 Marks				
		PART A -	$(6 \times 1 = 6 \text{ Marks})$				
	(Answe	r any six o	of the following ques	tions)			
1.	ARM processors are basical						
	(a) Main frame systems		(b) Distributed systems				
	(c) Mobile systems		(d) Super computers				
2.	ARM7 is a processor	with	Architecture				
	(a) RISC, Harvard	PART A nswer any six of sically designer ems essor with mann mpressed into a generation is can (b) Loader	(b) C	ISC, Von Neumann			
(c) RISC, Von Neumann			(d) CISC, Hardvard				
3. A large memory is compressed into a small one by using							
(a) LSI semiconductor			(b)VLSI semiconductor				
	(c) CDR semiconductor		(d) MSI semiconductor				
4. Executable binary file generation is carried out by							
	(a) Assembler (b)	Loader	(c) Linker	(d) Compiler			
5.	If the period of process is F	then the r	ate of the task is				

(c) 1/P

(d) P

(b) 2P

(a) P²

6.	The priorities that change	durin	g execution is					
	(a) Static	Static (b) Dynamic		(c) Both	(d) None			
7.	The interconnect network	he interconnect network used in automotive electronics is						
	(a) I^2C	(b) Ethernet		(c) Internet	(d) CAN			
8.	Internet enabled network	nternet enabled network has applications in						
	(a) Hard Real time	(b) Soft Real Time		(c) In both a & b	(d) Non Real Time			
9.	Software Modem utilizes							
	(a) PSK	(b)	ASK	(c) FSK	(d) QPSK			
10.	Huffman coding is used f	or						
	(a) Text compression (b) Video compression							
	(c) Image compression		(d) File compression					
		PA	$RT - B (3 \times 8 =$	24 Marks)				
(Answer any three of the following questions)								
11.	. Explain about cache memory in ARM processor.							
12.	2. Explain on how on chip memory management schemes can improve higher spee process. (8)							
13.	. Describe in detail about the inter process communication mechanism.							
14.	. Explain briefly I ² C bus and Ethernet.							
15.	Explain the design requirements.	proce	edure of data	compressor with i	-	and (8)		