Reg. No. : | | | | | | | | | | |

Question Paper Code: 49403

B.E. / B.Tech. DEGREE EXAMINATION, DEC 2020

Elective

Electronics and Communication Engineering

14UEC903 - COMPUTER ARCHITECTURE AND ORGANIZATION

(Regulation 2014)

Duration: 1.15 hrs Maximum: 30 Marks

PART A - (6 x 1 = 6 Marks)

(Answer any six of the following questions)

1. The addressing mode which makes use of in-direction pointers is

   (a) Indirect addressing mode (b) Index addressing mode

   (c) Relative addressing mode (d) Offset addressing mode

2. Floating point representation is used to store

   (a) boolean values (b) whole numbers
   (c) real integers (d) integers

3. In computers, subtraction is generally carried out by

   (a) 9's complement (b) 10's complement
   (c) 1's complement (d) 2's complement

4. Pipeline implement

   (a) fetch instruction (b) decode instruction
   (c) fetch operand (d) calculate operand

5. CPU does not perform the operation

   (a) data transfer (b) logic operation

   (c) arithmetic operation (d) all the above

6. A micro program written as string of 0's and 1's is a

(a) symbolic microinstruction (b) binary microinstruction

(c) symbolic micro program (d) binary micro program

7. The techniques which move the program blocks to or from the physical memory is called as

(a) Paging (b) Virtual memory organization

(c) Overlays (d) Framing

8. The associatively mapped virtual memory makes use of

(a) Translation Look-aside Buffer (b) Page table

(c) Frame table (d) None of these

9. The computer architecture aimed at reducing the time of execution of instructions is

(a) CISC (b) RISC (c) ISA (d) ANNA

10. Interrupts which are initiated by an instruction are

(a) internal (b) external (c) hardware (d) software

PART – B (3 x 8= 24 Marks)

(Answer any three of the following questions)

11. What are the different types of CPU organization? Explain with relevant examples. (8)

12. With relevant diagram and expressions, explain the operation of carry look ahead adder. (8)

13. Explain the design of micro programmed control unit with relevant diagram. (8)

14 Explain preemptive and non-preemptive memory allocation strategies in detail. (8)

15 Explain the IOB organization and communication between CPU and IOB. (8)