Reg. No. :

Question Paper Code: 39403

B.E. / B.Tech. DEGREE EXAMINATION, DEC 2020

Elective

Electronics and Communication Engineering

01UEC903 - COMPUTER ARCHITECTURE AND ORGANIZATION

(Regulation 2013)

Duration: 1.15 hrs   Maximum: 30 Marks

PART A - (6 x 1 = 6 Marks)

(Answer any six of the following questions)

1. The addressing mode which makes use of in-direction pointers is

    (a) Indirect addressing mode   (b) Index addressing mode

    (c) Relative addressing mode   (d) Offset addressing mode

2. Floating point representation is used to store

    (a) boolean values   (b) whole numbers
    (c) real integers   (d) integers

3. In computers, subtraction is generally carried out by

    (a) 9's complement   (b) 10's complement

    (c) 1's complement   (d) 2's complement

4. Pipeline implement

    (a) fetch instruction   (b) decode instruction
    (c) fetch operand   (d) calculate operand

5. CPU does not perform the operation

    (a) data transfer   (b) logic operation

    (c) arithmetic operation   (d) all the above

6. A micro program written as string of 0's and 1's is a

    (a) symbolic microinstruction   (b) binary microinstruction

    (c) symbolic micro program   (d) binary micro program

7. The techniques which move the program blocks to or from the physical memory is called as

    (a) Paging   (b) Virtual memory organization

    (c) Overlays   (d) Framing

8. The associatively mapped virtual memory makes use of

    (a) Translation Look-aside Buffer   (b) Page table

    (c) Frame table   (d) None of these

9. The computer architecture aimed at reducing the time of execution of instructions is

    (a) CISC   (b) RISC   (c) ISA   (d) ANNA

10. Interrupts which are initiated by an instruction are

    (a) internal   (b) external   (c) hardware   (d) software

PART – B (3 x 8= 24 Marks)

(Answer any three of the following questions)

11.   Explain zero, one, two and three addressing instructions with example.   (8)

12.   With a neat block diagram explain in detail about CPU-coprocessor interfacing.

    (8)

13.   Explain the design of micro-programmed control unit for the two's complement multiplier with a diagram.   (8)

14.   Design the following RAM using N x w bit IC RAM.

        (1) N x 4w bit RAM

        (2) 4N x w bit RAM   (8)

15.   With a diagram explain static and dynamic redundancy for designing fault tolerant system.   (8)

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