**Reg. No. :** | | | | | | | | | | |

## Question Paper Code: 47504

B.E. / B.Tech. DEGREE EXAMINATION, DEC 2020

Seventh Semester

Electronics and Instrumentation Engineering

14UEI704 - VLSI SYSTEM DESIGN

(Regulation 2014)

Duration: One hour Maximum: 30 Marks

PART A - (6 x 1 = 6 Marks)

**(Answer any six of the following questions)**

1. nMOS devices are formed in

   (a) p-type substrate of high doping level (b) n-type substrate of low doping level

   (c) p-type substrate of moderate doping level (d) n-type substrate of high doping level

2. Source and drain in nMOS device are isolated by

   (a) A single diode (b) Two diodes (c) Three diodes (d) Four diodes

3. If n-transistor conducts and has large voltage between source and drain, then it is said to be in _____ region

   (a) Linear (b) Saturation (c) Non saturation (d) Non saturation

4. In basic inverter circuit, _____ is connected to ground

   (a) Source (b) Gates (c) Drain (d) Resistance

5. In dynamic CMOS logic _____ is used

   (a) Two phase clock (b) Three phase clock
   (c) One phase clock (d) Four phase clock

6. Which multiplier is very well suited for twos complement numebers?

(a) Baugh-wooley algorithm (b) Wallace trees

(c) Dadda multipliers (d) Modified booth encoding

7. PAL has

(a) Programmable AND array and a fixed OR array

(b) Programmable OR array and a fixed AND array

(c) Programmable AND and OR array

(d) All the above

8. Which type of device FPGA are?

(a) SLD (b) SROM (c) EPROM (d) PLD back

9. What do VHDL stand for?

(a) Verilog hardware description language (b) VHSIC hardware description language

(c) very hardware description language (d) VMEbus description language

10. In VHDL, which class of scalar data type represents the values necessary for a specific operation?

(a) Integer types (b) Real types (c) Physical type (d) Enumerated types

PART – B (3 x 8= 24 Marks)

**(Answer any three of the following questions)**

11. Explain in detail about MOS transistor with the working operation of enhancement mode and depletion mode.. (8)

12. Describe the base operation of nMOS inverter. Also determine the pull-up to pull down ratio for an nMOS inverter driven through one or more pass transistors. (8)

13. Design a $2^s$ complement multiplication using Baugh Wooley method (8)

14. Write short notes on floor planning, placement and routing of FPGA. Also explain with a neat FPGA architecture. (8)

15. Write VHDL testbench code for 4:1 multiplexer. (8)