Reg. No. : | | | | | | | | | | |

Question Paper Code: 37504

B.E. / B.Tech. DEGREE EXAMINATION, DEC 2020

Seventh Semester

Electronics and Instrumentation Engineering

01UEI704 - VLSI SYSTEM DESIGN

(Regulation 2013)

Duration: One hour Maximum: 30 Marks

PART A - (6 x 1 = 6 Marks)

(Answer any six of the following questions)

1. nMOS devices are formed in

   (a) p-type substrate of high doping level (b) n-type substrate of low doping level

   (c) p-type substrate of moderate doping level (d) n-type substrate of high doping level

2. Source and drain in nMOS device are isolated by

   (a) A single diode (b) Two diodes (c) Three diodes (d) Four diodes

3. If n-transistor conducts and has large voltage between source and drain, then it is said to be in _____ region

   (a) Linear (b) Saturation (c) Non saturation (d) Non saturation

4. In basic inverter circuit, _____ is connected to ground

   (a) Source (b) Gates (c) Drain (d) Resistance

5. In dynamic CMOS logic _____ is used

   (a) Two phase clock (b) Three phase clock
   (c) One phase clock (d) Four phase clock

6. Which multiplier is very well suited for twos complement numebers?

(a) Baugh-wooley algorithm (b) Wallace trees

(c) Dadda multipliers (d) Modified booth encoding

7. PAL has

(a) Programmable AND array and a fixed OR array

(b) Programmable OR array and a fixed AND array

(c) Programmable AND and OR array

(d) All the above

8. Which type of device FPGA are?

(a) SLD (b) SROM (c) EPROM (d) PLD back

9. What do VHDL stand for?

(a) Verilog hardware description language (b) VHSIC hardware description language

(c) very hardware description language (d) VMEbus description language

10. In VHDL, which class of scalar data type represents the values necessary for a specific operation?

(a) Integer types (b) Real types (c) Physical type (d) Enumerated types

PART – B (3 x 8= 24 Marks)

(Answer any three of the following questions)

11. Show the various components of nMOS transistor model. (8)

12. Explain the DC characteristics and switching characteristics of a CMOS inverter. (8)

13. What is Barrel shifter and discuss its SHIFT-1 and SHIEFT-2 operation. (8)

14. Explain the NMOS NAND-NAND PLA realization with a neat stick diagram. (8)

15. Explain a simple test bench for any one Flip-Flop with necessary VHDL code. (8)