C

Reg. No. :

Question Paper Code: 53R01

M.E. DEGREE EXAMINATION, NOV 2019

Third Semester

Computer Science and Engineering

15PCS301 - MULTI CORE ARCHITECTURE

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART - A (5 x 1= 5 Marks)

1. Deeply pipelined circuits are having CO1- R

   (a) Heat Problems (b) Clock Problems

   (c) Efficiency Problems (d) Both (a) & (b)

2. Initially: If Flag1 = Flag2 = 0 then p1 , p2 are having critical section as CO2 -R

   (a) (1,0) (b) (0,1) (c) (0,0) (d) (1,1)

3. The Memory Address register stores the address of the word stored in which part of the architecture? CO3- R

   (a) I/O (b) Program Counter

   (c) Memory Buffer Register (d) None of the above

4. Design of memory hierarchy determines CO4 -R

   (a) Each level of memory development (b) Design of memory

   (c) Characteristics of memory design (d) None of the above

5. Parallel programming models is also called as CO5- R

   (a) Symmetric analysis model (b) Asymmetric analysis model

   (c) Bipolar model (d) None of the above

PART – B (5 x 3= 15Marks)

6.	What is mean by Hardware & Software Exploitation?	CO1-U	
7.	What are the different types of issues in Multiprocessor?	CO2-U	
8.	Compare the features of Homogenous& Heterogeneous Architectures.	CO3-Ana	
9.	List out the optimization techniques for memory.	CO4-U	
10.	What is mean by shared programming models?	CO5-U	

PART – C (5 x 16= 80Marks)

11.	(a)	Implement the concept of Multithreading in parallelism.	CO1- U	(16)
		Or		
	(b)	What is ILP? Explain its exploitation.	CO1- U	(16)
12.	(a)	Explain in detail the distributed shared memory architecture highlighting the directory based cache coherence protocol. Justify your explanation with suitable examples and state diagrams.	CO2- E	(16)
		Or		
	(b)	Explain how thread level parallelism within a processor can be exploited? With suitable diagrams, explain simultaneous multithreading, its design challenges and potential performance enhancements.	CO2- E	(16)
13.	(a)	Compare the features and relate the connections between the Intel & SUN CMP Architecture.	CO3-Ana	(16)
		Or		
	(b)	Implement the concept of heterogeneous architecture in the multi-processing issues.	CO3-Ana	(16)
14.	(a)	Illustrate the designing methodologies that involved in the memory hierarchy.	CO4 -U	(16)
		Or		
	(b)	Describe the concept of virtual memory & virtual machines.	CO4 -U	(16)
15.	(a)	Design a open mp program for thread creation & initialization.	CO5-U	(16)
		Or		
	(b)	What are the different types of message passing interface methods and explain in detail.	CO5-U	(16)